# A Low-leakage Current Power 180-nm CMOS SRAM

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**Abstract - A low leakage power, 180-nm 1K-b SRAM was fabricated. The stand-by leakage power of a 1K-bit memory cell array incorporating a newly-developed leakage current reduction circuit called a "Self-controllable Voltage Level (SVL)" circuit was only 3.7nW, which is 5.4% that of an equivalent conventional memory-cell array at a $V_{DD}$ of 1.8V. On the other hand, the speed remained almost constant with a minimal overhead in terms of the memory cell array area.**

## I. Introduction

Battery-driven portable systems need low leakage power techniques. There are two well-known techniques that reduce leakage power ($P_{ST}$). One is to use a multi-threshold-voltage CMOS (MTCMOS) [1]. It effectively reduces $P_{ST}$ by disconnecting the power supply through the use of high $V_t$ MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) [2] that reduces $P_{ST}$ by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits.

To solve the above-mentioned drawbacks, a small leakage current reduction circuit called a Self-controllable Voltage Level (SVL) circuit has been developed that not only significantly decreases $P_{ST}$, but also retains data during a stand-by period. We applied this technique to a 1K-bit 180-nm SRAM that could potentially be used in future multimedia mobile applications to examine the effects of the SVL circuit on the $P_{ST}$ of storage circuits.

## II. Circuit Design, Fabrication, and Characteristics

### 2.1 "Self-controllable Voltage Level (SVL)" Circuit

The SVL circuit consists of an upper SVL (U-SVL) circuit and a lower SVL (L-SVL) circuit (Fig. 1), where a single inverter has been used as the load circuit. The SVL circuit shown in Fig. 2 is applied to the SRAM memory cell array. The U-SVL circuit is constructed of a wide channel pull-up pMOSFET switch (pSW) and multiple nMOSFET resistors (nRS*m*; *m*=1, 2,•••) connected in series. Similarly, the L-SVL circuit incorporates a wide channel pull-down nMOSFET switch (nSW) and multiple series-connected pMOSFET resistors (pRS*m*).

While the load circuit is active (i.e., *CLB*="0" and *CL*="1"), both the pSW and nSW are turned on, but the nRS1 and pRS1 are turned off. Therefore, the U-SVL and L-SVL circuits can supply a maximum supply voltage $V_D$ (=$V_{DD}$) and a minimum ground-level voltage $V_S$ (=$V_{SS}$=0), respectively, to the active load circuit. Thus, the operating speed of the load circuit can be maximized.

When the load circuit is in stand-by (i.e., *CLB*="1" and *CL*="0"), all the nRS*m* and pRS*m* switches are turned on, and both the pSW and nSW are turned off. Thus, the U-SVL and L-SVL circuits respectively generate a slightly lower supply voltage $V_D$ (=$V_{DD}$-$v_n$<$V_{DD}$) and a relatively higher "ground-level" voltage $V_S$ (=$v_p$>0V), where $v_n$ and $v_p$ are the total voltage drops of all nRS*m* and all pRS*m*, respectively. Thus, the back-gate biases ($V_{BG}$s) {i.e., source voltages ($V_s$)} of both the "cut-off" pMOSFETs and the nMOSFETs in the stand-by load circuit are increased and are given by $v_n$ and -$v_p$, respectively.

The increase in $V_{BG}$s will increase the $V_t$s of the "cut-off" MOSFETs. Therefore, the leakage currents of the "cut-off" MOSFETs decrease.

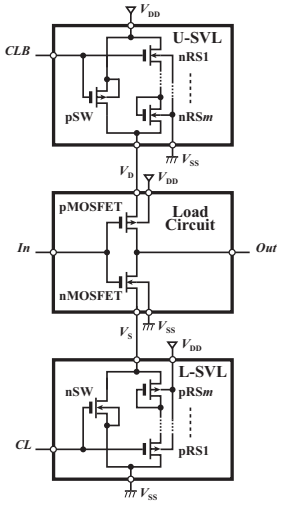


**Fig. 1. Leakage current reduction circuit, called a "Self-controllable Voltage Level (SVL)" circuit.**

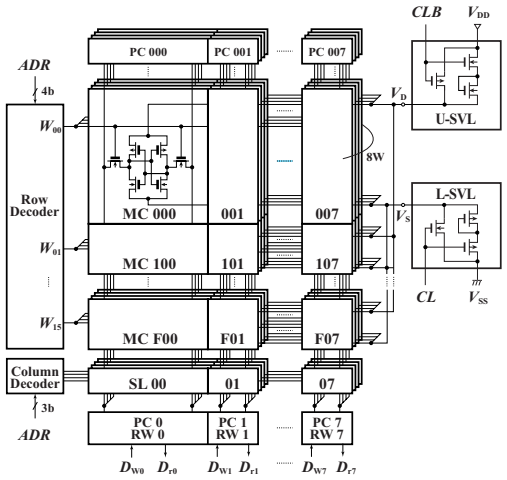


**Fig. 2. Circuit diagram of SRAM with 1K-bit memory-cell array incorporating SVL circuit with *m* of 2.**

Furthermore, the increase in $V_s$ increases the "write" operating margin [3]. Similarly, the $V_{ds}$s of the "cut-off" MOSFETs decreases and becomes $V_{DD}$-($v_n$+$v_p$). Decreasing $V_{ds}$ will decrease the effect of the drain-induced barrier lowering (DIBL) so that the leakage currents decrease even more. In addition, the SVL circuit not only reduces the $V_{gd}$ of the "cut-off" MOSFETs, but also reduces the $V_{gc}$ of the "turn-on" MOSFETs. Decreasing $V_{gd}$ reduces the GIDL currents of the "cut-off" MOSFETs and decreasing $V_{gc}$ decreases the gate-quantum-tunneling leakage currents of the "turn-on" MOSFETs. Therefore, the total leakage current of the load circuit will greatly decrease.

### 2.2 SRAM Design and Performance

We fabricated SRAMs with a 1K-bit (8b×8W×16W) memory-cell array incorporating an SVL circuit with an *m* of 1 or 2

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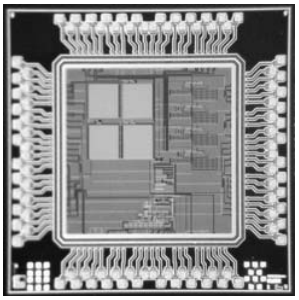

**Fig. 3. 180-nm CMOS LSI that includes SRAMs with 1K-bit memory-cell array incorporating SVL circuit.**

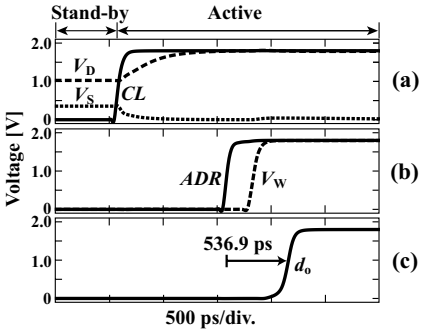


**Fig. 4. Simulated waveforms at several nodes in SRAM with 1K-bit memory-cell array with the SVL circuit ($m$=2).**

using 180-nm CMOS technology. A photograph of the SRAM LSI chip is shown in Fig. 3. The channel widths of the pMOSFETs and nMOSFETs in the memory cells are 2.5 µm and 1.25 µm, respectively, those of the pSW and nSW are 320 µm, and those of the pRS$m$ and nRS$m$ are 1.25 µm. Figure 4 shows the simulated voltage levels at various nodes in the SRAM with the 1K-bit memory-cell array incorporating the SVL circuit with an $m$ of 2. As shown in Fig. 4(a), the SVL circuit supplies a lower $V_D$ (1.03V) and a relatively higher $V_S$ (0.35V) to the memory cell array, and retains the memory cell data during stand-by. When $CL$ goes to a high level, $V_D$ increases to $V_{DD}$ (1.8V), while $V_S$ decreases to $V_{SS}$ (0V), so the SRAM becomes active within about 600 psec. Figure 4(b) shows the row address ($ADR$) and word-line voltage ($V_W$) waveforms, and Fig. 4(c) shows the output datum ($d_o$="1") waveform. The "read" access time of the new SRAM is 536.9 psec, namely, almost the same as that (535.5 psec) of the conventional 1K-bit SRAM.

Figure 5 depicts the measured stand-by power ($P_{STm1}$) of a 1K-bit memory-cell array based on an SVL circuit with an $m$ of 1, that ($P_{STm2}$) of a 1K-bit memory-cell array incorporating an SVL circuit with an $m$ of 2, and that ($P_{STcon}$) of the conventional memory cell array. Figure 5 also plots the stand-by power ratio. $P_{STm2}$ is drastically reduced to 3.7nW, which is namely 5.4% of the $P_{STcon}$ (=69.1nW) at $V_{DD}$=1.8 V.

Figure 6 shows the measured waveforms at various nodes of an SRAM with a 1K-bit memory-cell array incorporating an SVL circuit with an $m$ of 2. Figures 6 (a), (b), (c), and (d) are the 100-MHz clock ($clk$), Read/Write control signal ($WE$), "write data" ($d_i$s) and "read data" ($d_o$s), respectively.

The active power ($P_{AT}$) of an SRAM with a 1K-bit memory-cell array based on the SVL circuit with an $m$ of 2 at a clock frequency ($f_c$) of 200MHz and a $V_{DD}$ of 1.8V was 3.295mW, which was almost the same as that (3.296mW) of a conventional 1K-bit SRAM. Table 1 summarizes the characteristics of the 1K-bit, 180-nm CMOS SRAMs.

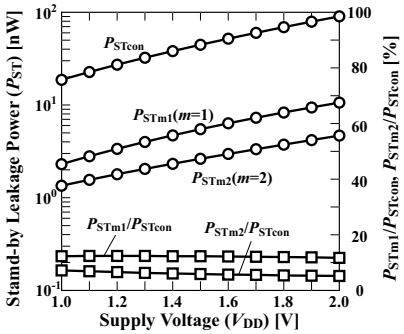


**Fig. 5. Measured stand-by leakage power ($P_{ST}$) as function of supply voltage ($V_{DD}$).**

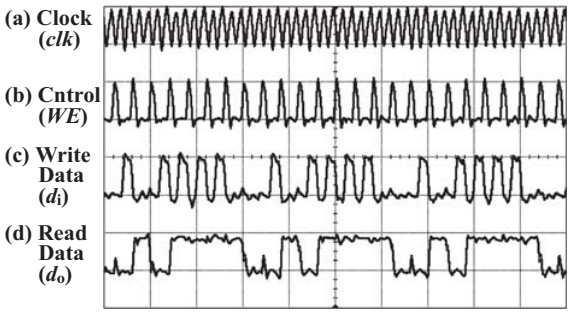


**Fig. 6. Measured waveforms at various nodes in 180-nm SRAM with 1K-bit memory-cell array incorporating SVL circuit with $m$ of 2 ($f_c$=100MHz, $V_{DD}$=1.8V, and $V_{SS}$=0V).**

**Table 1. Characteristics of 1K-bit, 180-nm CMOS SRAMs ($V_{DD}$=1.8V and $V_{SS}$=0V).**

| | Conv. | SVL circuit $m$=1 | SVL circuit $m$=2 |
|---|---|---|---|
| $P_{ST}$ of memory cell array [nW] | 69.1 (100%) | 8.3 (12%) | 3.7 (5.4%) |
| "1" "read" access time [psec] | 535.5 (100%) | 536.9 (100.3%) | 536.9 (100.3%) |
| Memory cell array area [mm$^2$] | 0.0944 (100%) | 0.0959 (101.6%) | 0.0960 (101.7%) |

## III. Conclusion

We fabricated 1K-b SRAMs with a leakage current reduction circuit using a 180-nm CMOS process. The measured stand-by leakage power of the 1K-b SRAM memory cell array significantly decreased to 5.4% that of the conventional SRAM memory cell array, while the speed degradation and area overhead were negligible and the "write" operating margin was increased.

We concluded that the developed SRAM incorporating the SVL circuit, which can retain data even in stand-by, will play a major role in future deep sub-100-nm CMOS SRAMs.

## References

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