ASP-DAC 2007 Technical Program Committee

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Subcommittees (∗ indicates the subcommitte chair.)

[1] System Level Design

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Jean Christophe Madre
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Tsuneo Nakata
Fujitsu Lab.

[2] Embedded and Real-Time Systems

∗**Hiroyuki Tomiyama**
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Yonsei Univ.
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Matsushita Electric Industrial Co.
Tei-Wei Kuo
National Taiwan Univ.
Yunheung Paek
Seoul National Univ.
Sri Parameswaran
Univ. of New South Wales

[3] Behavioral/Logic Synthesis and Optimization

∗**Shinji Kimura**
Waseda Univ.
Shih-Chieh Chang
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Deming Chen
Univ. of Illinois, Urbana-Champaign
Ki-seok Chung
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Diana Marculescu
Carnegie Mellon Univ.
Shigeru Yamashita
NAIST

[4] Validation and Verification for Behavioral/Logic Design

∗**Karem Sakallah**
Univ. of Michigan
Jin-Young Choi
Korea Univ.
Thomas Kropf
Bosch
Pete Manolios
Georgia Tech.
Shin'ichi Minato
Hokkaido Univ.
John Moondanos
Intel
Jun Sawada
IBM

[5] Physical Design (Routing)

∗**Martin D. F. Wong**
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Charles Chiang
Synopsys (China)
Hyunchul Shin
Hanyang Univ.
Atsushi Takahashi
Tokyo Inst. of Tech.
Ting-Chi Wang
National Tsing Hua Univ.

[6] Physical Design (Placement)

∗**Yao-Wen Chang**
National Taiwan Univ.
Hung-Ming Chen
National Chiao Tung Univ.
Shigetoshi Nakatake
Univ. of Kitakyushu
Gi-Joon Nam
IBM
David Pan
Univ. of Texas at Austin
Jens Vygen
Univ. of Bonn
Shin'ichi Wakabayashi
Hiroshima City Univ.

[7] Timing, Power, Signal/Power Integrity Analysis and Optimization

∗**Sachin Sapatnekar**
Univ. of Minnesota
Shabbir Batterywala
Synopsys (India)
Hongliang Chang
Cadence
Masanori Hashimoto
Osaka Univ.
Jin-Jia Liou
National Tsing Hua Univ.
Frank Liu
IBM
Youngsoo Shin
KAIST

[8] Interconnect, Device and Circuit Modeling and Simulation

∗**Hideki Asai**
Shizuoka Univ.
Arun Chandrasekhar
Intel (India)
Charlie Chung-Ping Chen
National Taiwan Univ.
Yungseon Eo
Hanyang Univ.
Takashi Sato
Tokyo Inst. of Tech.
Sheldon Tan
Univ. of California, Riverside
Yu Wenjian
Tsinghua Univ.

[9] Test and Design for Testability

∗**Seiji Kajihara**
Kyushu Inst. of Tech.
Kuen-Jong Lee
National Cheng Kung Univ.
XiaoWei Li
China Academy of Sciences
Satoshi Ohtake
NAIST
Prab Varma
Blue Pearl

[10] Analog, RF and Mixed Signal Design and CAD

∗**Jaijeet Roychowdhury**
Univ. of Minnesota
Brian Otis
Univ. of Washington
Zhiping Yu
Tsinghua Univ.
SeongHwan Cho
KAIST
Chau-Chin Su
National Chao-Tung Univ.
Tomohisa Kimura
Toshiba
Inoue Yasuaki
Waseda Univ.

[11] Leading Edge Design Methodology for SOCs and SIPs

∗**Hideharu Amano**
Keio Univ.
Shorin Kyo
NEC
Yulu Yang
Nankai Univ.
Ing-Jer Huang
National Sun-Yat-Sen Univ.
Seongsoo Lee
Soongsil Univ.
Takeshi Ikenaga
Waseda Univ.
Takashi Miyamori
Toshiba