ASP-DAC 2007 Best Papers

Best Paper Award

3B-2 **Protocol Transducer Synthesis using Divide and Conquer Approach**
Shota Watanabe, Kenshu Seto, Yuji Ishikawa, Satoshi Komatsu, Masahiro Fujita (Univ. of Tokyo, Japan)

5A-1 **A New Methodology for Interconnect Parasitics Extraction Considering Photo-Lithography Effects**
Ying Zhou (Texas A&M Univ., United States), Zhuo Li (Pextra Corp., United States), Yuxin Tian, Weiping Shi (Texas A&M Univ., United States), Frank Liu (IBM, United States)

Best Paper Candidates

1C-1 **A New Boundary Element Method for Multiple-Frequency Parameter Extraction of Lossy Substrates**
Xiren Wang, Wenjian Yu, Zeyi Wang (Tsinghua Univ., China)

2A-1 **Fast Analytic Placement using Minimum Cost Flow**
Ameya R Agnihotri, Patrick H Madden (SUNY Binghamton, United States)

3A-1 **A Novel Performance-Driven Topology Design Algorithm**
Min Pan, Chris Chu (Iowa State Univ., United States), Priyadarsan Patra (Intel Co., United States)

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6C-1 **Improving XOR-Dominated Circuits by Exploiting Dependencies between Operands**
Ajay K. Verma, Paolo Ienne (Ecole Polytechnique Federale de Lausanne, Switzerland)

7A-2 **Runtime Leakage Power Estimation Technique for Combinational Circuits**
Yu-Shiang Lin, Dennis Sylvester (Univ. of Michigan, United States)

7C-1 **Shelf Packing to the Design and Optimization of a Power-Aware Multi-Frequency Wrapper Architecture for Modular IP Cores**
Danella Zhao, Unni Chandran (Univ. of Louisiana, Lafayette, United States), Hideo Fujiwara (NAIST, Japan)

9B-1 **Design Methodology for 2.4GHz Dual-Core Microprocessor**
Noriyuki Ito, Hiroaki Komatsu, Akira Kanuma, Akihiro Yoshitake, Yoshiyasu Tanamura, Hiroyuki Sugiyama, Ryoichi Yamashita, Ken-ichi Nabeya, Hironobu Yoshino, Hitoshi Yamanaka, Masahiro Yanagida, Yoshitomo Ozeki, Kinya Ishizaka, Takeshi Kono, Yutaka Isoda (Fujitsu Ltd., Japan)

Design Contest Award

Outstanding Design Award

1D-1 **A 1Tb/s 3W Inductive-Coupling Transceiver Chip**
Noriyuki Miura, Tadahiro Kuroda (Keio Univ., Japan)

Special Feature Award

1D-9 **Improving Execution Speed of FPGA using Dynamically Reconfigurable Technique**
Roel Pantonial, Md. Ashfaquzzaman Khan, Naoto Miyamoto, Koji Kotani, Shigetoshi Sugawa, Tadahiro Ohmi (Tohoku Univ., Japan)

1D-13 **Implementation of a Standby-Power-Free CAM Based on Complementary Ferroelectric-Capacitor Logic**
Shoun Matsunaga, Takahiro Hanyu (Tohoku Univ., Japan), Hiromitsu Kimura, Takashi Nakamura, Hidemi Takasu (ROHM, Japan)