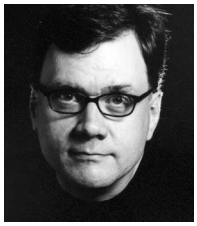
Keynote Address I

Next-Generation Design and EDA Challenges: Small Physics, Big Systems, and Tall Tool-Chains



Rob A. Rutenbar

Electrical & Computer Engineering, Carnegie Mellon University, United States

There is much discussion of two challenges in the design of tomorrow's electronics: the difficult "small physics" of nanoscale transistors, and the silicon/software complexity of "big systems". But those of us who want to build beautiful algorithms have an additional hurdle: "tall tool-chains". If it takes 50 tool-steps to build an industrial-strength design flow, and each tool is based on 1-2 "big algorithms", does this mean that each new algorithm idea is worth, at best, 1-2% of the success of a design? This seems to me a bad way of accounting for the tremendous value that EDA brings to the world of design. How can we have a big impact in this important technology area?

In this talk, I will offer several pieces of advice for how not to get buried by the tall-tool-chain problem. I will discuss how to identify design problems that can have large impact, how to embrace the strange physics of tomorrow's silicon technologies in the service of building beautiful algorithms, and how to get fresh (and unique) insights on problems by spending time working with a real design team. I will use design examples ranging from lithography, to computational finance, to silicon-based speech recognition, to illustrate the point that this is an exciting time to be working on tomorrow's tool and design challenges.

Keynote Address II

Meeting with the Forthcoming IC Design — The Era of Power, Variability and NRE Explosion and a Bit of the Future —

Takayasu Sakurai

Center for Collaborative Research, and Institute of Industrial Science, University of Tokyo, Japan

In the foreseeable future, VLSI design will meet a couple of explosions: power, variability and NRE (non-recurring engineering cost). Some of the solutions for power-aware designs are covered in this talk with relation to variability. A remedy for the NRE explosion is to reduce the number of developments and manufacture and sell tens of millions of chips under a fixed design. System-in-a-Package approach may embody such possibility. Several new technologies are described to enable 3-dimensional stacking of chips to build high-performance yet low-power electronics systems.

On the other extreme of the silicon VLSI's which stay as small as a centimeter square, a new domain of electronics called large-area integrated circuit as large as meters is waiting, which may open up a new continent of applications in the era of ubiquitous electronics. One of the implementations of the large-area electronics is based on organic transistors. The talk will provide perspectives of the organic circuit design taking E-skin, sheet-type scanner and Braille display as examples.

Keynote Address III

How Foundry can Help Improve your Bottom-Line? Accuracy Matters!

Fu-Chieh Hsu

Vice President of Design and
Technology Platform
Taiwan Semiconductor Manufacturing Company, Taiwan

As the leading edge of technology advances into the nanometer era, process data accuracy becomes increasingly important to the success of product designs. The gap between theoretical benefit and benefit obtainable by designers grows wider with each new technology node. However, foundries and EDA tool vendors can collaborate to reclaim some of the lost benefits of these technology nodes.

In this talk, I will discuss how foundries can contribute in the effort to reclaim lost benefits through better model and data accuracy, while EDA tool vendors contribute through improved design approaches. I will give some examples of TSMC's approaches in improving SPICE model accuracy and DFM accuracy, as well as collaboration with EDA tool vendors in creating our DFM Data Kit. By increasing awareness of TSMC's approach to this issue, I hope to stimulate discussion from all sides of the industry in the search for more solutions.