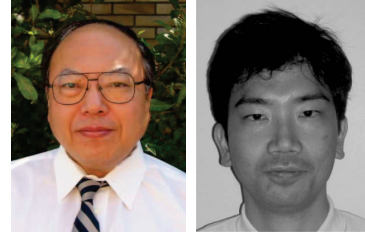


Designers' Forum

Designers' Forum is conceived as a unique program that shares design experience and solutions of real product designs of the industries among LSI/PCB designers and EDA academia/developers. It consists of these four special sessions.

- Oral Sessions
 - 6D High-speed Chip to Chip Signaling Solutions
 - 8D Low-power SoC Technologies
- Panel Discussions:
 - 5D Presilicon SoC HW/SW Verification
 - 9D Top 10 Design Issues



Haruyuki Tago Kazutoshi Kobayashi

Here, designs will be presented focusing on design styles, design issues, and ways to tackle design issues. Panel discussions will also be held for the latest design issues. Detailed information of each session is as follows.

Session 6D (16:00-17:50, Jan 25th) [Low-power SoC Technologies] — This session deals with brand-new low-power SoC technologies for mobile digital consumer electronics. 3 presentation will be shown from Renesas, Toshiba and Matsushita. Renesas introduces a dedicated multimedia hardware embedded on SH-mobile. Toshiba shows a digital-TV decoder based on a configurable processor “MeP”. Matsushita introduces miscellaneous low power technologies on an SoC Platform called “Uniphier”.

Session 8D (13:30-15:35, Jan 26th) [High-speed Chip to Chip Signaling Solutions] — 4 presentations will be shown related to board or system level designs on PCs, games and servers given by Elpida, IBM, Fujitsu Lab. and Rambus. Elpida shows a 9.6Gbps FB-DiMM interface technology. IBM overviews a 21.6Gbps interface design on Xbox360. Fujitsu Lab. introduces a 6.25Gbps cable link for servers. Rambus describes a 3.2Gbps XDR memory system for the Cell processor.

Session 5D (13:30-15:35, Jan 25th) [Presilicon SoC HW/SW Verification] — Panelists discuss with verification technologies on system levels including hardwares and softwares prior to LSI fabrication. Three panelists are LSI designers for digital TV application and two panelists are from EDA vendors, The point of discussion is how to develop software using emulators, co-simulation and other technologies.

Session 9D (16:00-18:05, Jan 26th) [Top10 Design Issues] — Panelists will focus on the top 10 design issues seen by LSI designers and EDA vendors.



Designers' Forum Chair
Haruyuki Tago
Toshiba Corporation



Designers' Forum Vice Chair
Kazutoshi Kobayashi
Kyoto University