# A 2.8-V Multibit Complex Bandpass ΔΣAD Modulator in 0.18$\mu$m CMOS

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**Abstract— A second-order multibit switched-capacitor (SC) complex bandpass ΔΣAD modulator has been designed, fabricated and tested for application to low-IF receivers in wireless communication systems. We have employed two new algorithms there to improve the signal-to-noise-and-distortion (SNDR) of the modulator. (i) A complex bandpass filter with I, Q dynamic matching to reduce the mismatch influence between I, Q paths. As its by-product, the complex modulator can be divided into two separate parts without signal line crossing between the upper and lower paths. Therefore, the layout design of the modulator can be greatly simplified; (ii) A new complex bandpass Data-Weighted Averaging (DWA) algorithm is implemented to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy. Implemented in a 0.18-$\mu$m CMOS process and at 2.8V supply, the modulator achieves a measured peak SNDR of 64.5dB at 20MS/s with a signal bandwidth of 78kHz while dissipating 28.4mW and occupying an area of 1.82mm$^2$.**

## I. Introduction

A complex bandpass ΔΣAD modulator performs AD conversion only for the positive frequency of I, Q input signals in a low-IF receiver [1], and hence it can be realized with lower power dissipation than a pair of real bandpass ΔΣAD modulators which perform AD conversion for the negative frequency (image signal) as well as the positive frequency [2]. A multibit ΔΣAD modulator makes higher SNDR possibly to be with low-order loop filter, and the stability problem is alleviated. It is attractive for low power implementation because it alleviates the slew-rate requirements of OP-Amps with high dynamic range in the modulator. However, multibit DACs cannot be made perfectly linear and their nonlinearity in the feedback paths degrade the SNDR of the ΔΣAD modulator. Then we developed a DWA algorithm for complex bandpass modulator to suppress nonlinearity effects of multibit DACs in a complex form. Furthermore, we propose a new structure for a complex bandpass ΔΣAD modulator which can be divided into two separate paths without crossing signal lines between the upper and lower paths, and its layout design can be simplified. This paper presents the chip implementation with SC circuits employing the above-mentioned two algorithms. Measured results of the implemented chip show that above two algorithms are effective.

## II. Complex ΔΣ Modulator architecture

### A. New Structure of Complex Bandpass Filter

Fig.1(a) shows a basic complex bandpass filter while Fig.1(b) shows its proposed equivalent implementation, where four multiplexers (MUX) are added and their select signal (SEL) toggles at half rate of CLK in $z^{-1}$ block and they are synchronized. The proposed complex filter is divided into two separate parts without any crossing of signal lines. The input I and Q signals alternate between the upper and lower paths of the complex filter by SEL signal, so that it is equivalent to the conventional one when their circuits are ideal but the I, Q mismatch problem is alleviated [3].

### B. Complex Bandpass DWA Algorithm in Feedback Path

DACs in our modulator have 9-level resolution with the segmented SC architecture. Nonlinearities of the segmented DAC due to mismatches of capacitors introduce errors in feedback loop, and the SNDR of the modulator degrades. Fig.2 shows our proposed complex bandpass noise-shaping architecture, nonlinearities error of two DACs $e1 + je2$ can be noise shaped in a complex form at $f_s/4$. In practice, however, this structure cannot be realized because the input signals may be infinite (out-of-DAC-input-range). Then the equivalent implementation called complex DWA algorithm is proposed to realize the above architecture. Element selection logic circuits (DWA1 and DWA2) are added between the two ADC outputs and DAC inputs to select the DAC unit-elements in a rotational manner [4] as shown in Fig.3. For the I-channel and Q-channel DAC, we apply *highpass* and *lowpass* DWA algorithm with internal interaction between I, Q modulator output respectively. DAC1, DAC2 are used alternately for I, Q-channels, and hence mismatch effects between two DACs $e1 + je2$ are first-order complex bandpass noise-shaped at $f_s/4$.

## III. Circuit Implementation and Experimental Results

Fig.4 shows our entire proposed complex bandpass ΔΣAD modulator. It has no crossing signal lines for either the $z^{-1}$ block or the feedback paths from DACs. Hence its layout design can be greatly simplified, and its internal signal lines can be shorter, which leads to smaller chip area. The proposed modulator was designed with fully differential SC circuits, and the prototype is implemented in 0.18$\mu$m CMOS occupies $1.4 \times 1.3mm^2$, the chip micrograph is shown in Fig.5.

The degree of the mirror image signal suppression in the modulator was evaluated by demodulating the complex IF-signal down to baseband. The spectrum of the demodulated, complex valued baseband signal is shown in Fig.6 for a 4.92MHz sinusoidal input. The image signal is suppressed by 46 dB with respect to the desired signal, and measured peak SNDR is 64.5dB at 20MS/s. The modulator operates at 2.8V and consumes 28.4mW. Fig.7 shows output power spec-

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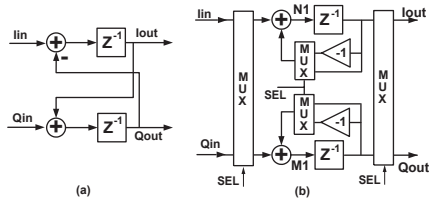


Fig. 1. (a) Basic complex bandpass filter. (b) Proposed equivalent implementation.

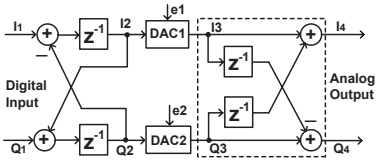


Fig. 2. Proposed architecture of DAC nonlinearitiy noise-shaping for a complex bandpass modulator. However, note that this architecture cannot be implemented directly.

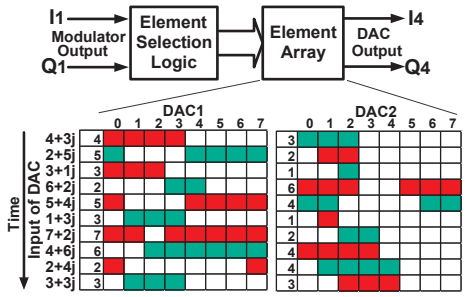


Fig. 3. Explanation of our complex bandpass DWA algorithm. The unit-current-cells in ON state are filled in black for a real part (I-path) and in gray for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

trum comparison of the modulator for zero input between at ON/OFF state of DWA logic. When DWA logic is at ON state, noise floor at the band of interest is about 3dB lower than that when DWA logic is at OFF state.

## Acknowledgements

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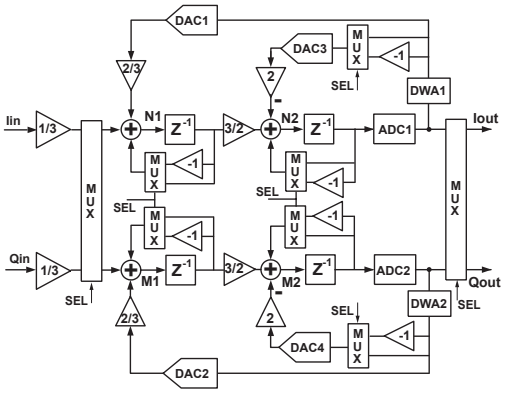


Fig. 4. Architecture of our complex bandpass ΔΣAD modulator.

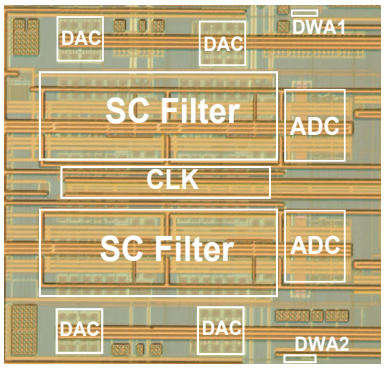


Fig. 5. Chip micrograph.

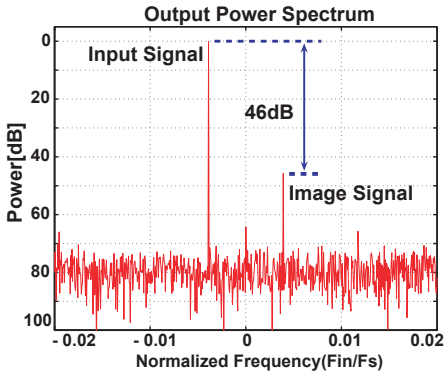


Fig. 6. Measured output power spectrum of the proposed modulator.

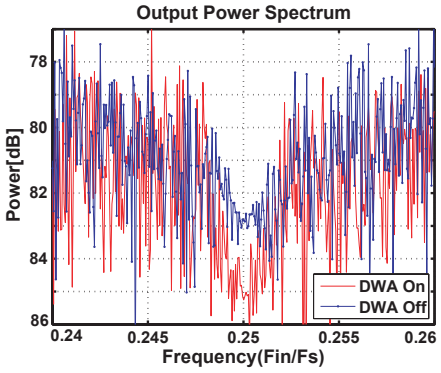


Fig. 7. Power spectrum comparison in cases of DWA on and off.