A Programmable Fully-Integrated GPS receiver in 0.18µm CMOS with Test Circuits

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Abstract — A 0.18µm single chip GPS receiver with 19.5 mA power consumption is implemented in 6.5 mm^2. A serial input digital control with additional testing structure not adding more than 4% to the Si area are used to the actual RF circuits in case of problems minimizing the number of Si runs.

***Index Terms* — Testability, Test Structure, CMOS Radio, Global Positioning System (GPS), Receiver.**

I. Introduction

The global positioning system (GPS) is a collection of satellites owned by the U.S. government that provides highly accurate, worldwide positioning and navigation information, 24 hours a day. It is made up of 24 NAVSTAR GPS satellites, Fig. 1, which orbit 12000 miles (about 20000 Km) above the Earth, constantly transmitting the precise time and their position in space. GPS receivers anywhere on (or near) the Earth's surface, listen in on the information received from three to twelve satellites and, from that, determine the precise location and time of the receiver, as well as how fast and in what direction it is moving.

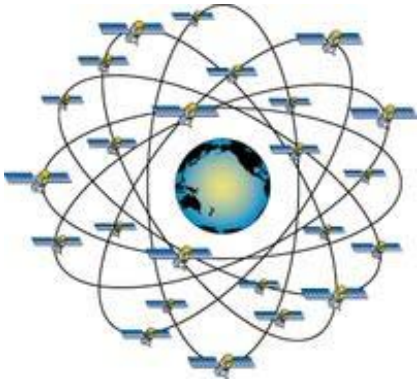

Fig. 1. GPS satellites constellation.

The GPS satellites broadcast signals in two 20-MHz-wide bands: the L1 band, centered at 1.57542 GHz, and the L2 band, centered at 1.2276 GHz. Both center frequencies are integer multiples of 10.23 MHz. Two direct-sequence spread spectrum signals are broadcast in these two bands. These are known as the P code (or precision code) and the C/A code (or coarse acquisition code). The P code, which is intended for military use, is broadcast in both bands, while the C/A code is broadcast only in the L1 band, see Fig 2. Note that the signal spectra of these two codes overlap.

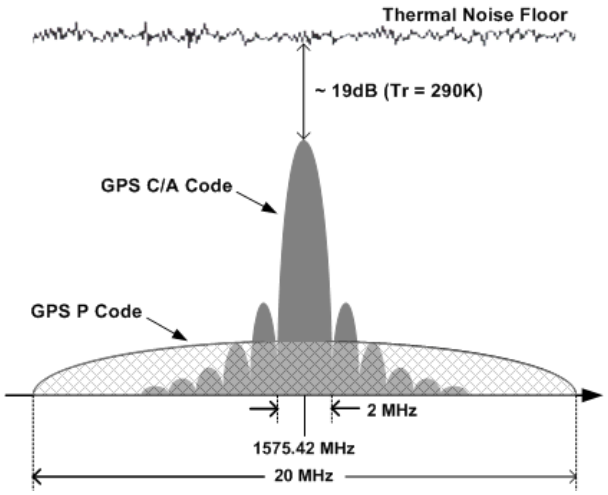

Fig. 2. The GPS L_1 band signal spectrum.

At the antenna of a GPS receiver, the received signal power is typically -130 dBm. Because we are interested in the 2- MHz main lobe of the C/A code, the noise power is simply given by $kTB \approx$ -111 dBm (T=290°K). Hence, the received signal-to-noise ratio (SNR) at the antenna is about -19 dB. The bit rate of the C/A code is only 50 bits/s. Thus, the processing gain is given by

$$G_P = 10\log\left(\frac{T_b}{T_c}\right) = 43\,dB \qquad (1)$$

Where T_b is the bit period of the C/A code and T_c is the chip period. So, with an antenna temperature of 290 K and an otherwise *noiseless* receiver, the postcorrelation SNR would be about 24 dB [5].

GPS has found its way to the consumer market. GPS systems are available in cars, watches, cell phones, etc. There is much recent research on integrating all CMOS transceivers systems on chip [1-5]. We designed a single-chip GPS receiver using 0.18µm CMOS. The receiver works in the GPS L-1 band at 1575.42MHz, which carries the C/A code.

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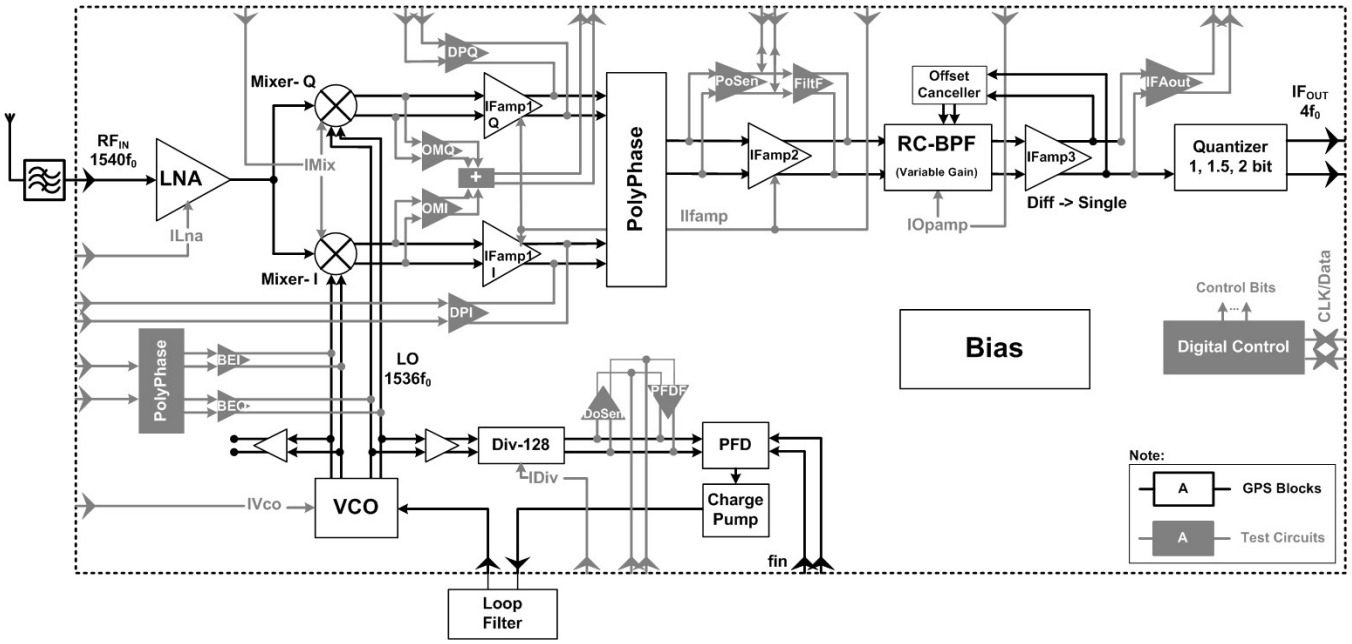


Fig 3. GPS receiver block diagram with the test circuits and test pins.

II. Architecture and Specifications

A low-IF architecture with 4MHz IF was chosen. The low-IF frequency guarantees a low energy at the image frequency and the feasibility of an integrated IF filter at a relatively low power consumption. With IF of 4MHz since the image-frequency of the C/A code lies in the P-code band, no other strong signals are present in this band and only 15dB image rejection is needed to limit the noise figure degradation due to image noise to less than 0.15dB [1]. Direct conversion and low-IF architecture are the most popular wireless receiver architecture today. Direct conversion avoids the problem of image frequency, but issues associated with low-frequency noise, DC offset and LO-leakage makes its implementation extremely difficult. Frequency planning of the proposed receiver is chosen to keep the reference clock harmonics and any wireless transmissions far away from the signal and image bands.

The front-end of the receiver is a quadrature low-IF receiver consisting of a low noise amplifier (LNA), image rejection using IQ mixers and passive polyphase filter. The IF path includes a programmable gain active band passed filter, two IF amplifiers, and a quantizer. The quadrature differential LO signals, switching two double-balanced mixers, are produced by the synthesizer block. The receiver uses only a few external passive components for the PLL loop filter. The non-grey blocks in Fig. 3 show the receiver architecture.

In analog circuit design, especially RF design, exact circuit models consisting of all parasitics are critical. Although the circuit models become more precise with time, RF/analog circuits must be taped out three, four or more times to achieve the final spec. We have designed a programmable GPS receiver with eight programming modes, one for normal operation and the others for testing the receiver blocks. The receiver modes were designed so as to test the circuit blocks in the closest possible condition to their actual operation instead of resorting to separate test structures that consume large Si areas (due to inductors). Therefore after the first tape out, all of the circuit problems could be recognized; hence minimum number of needed tape outs.

III. Receiver Path

A. RF Section

The GPS input signal is applied to a common source configuration LNA with inductive degeneration providing high voltage gain, low noise figure, and sufficient linearity. A single-ended LNA has been preferred to a balanced one to reduce power consumption and silicon area. Substrate noise has been eliminated using deep N-Well. The cascade configuration increases the LNA gain, reduces the effect of Miller capacitance, and increases the LNA reverse isolation. In the LNA circuit (Fig. 4), R_1 is used for dc biasing and C_1 for by-passing, L_g controls the gain and noise matching, C_2 effects on the input matching and noise figure, L_L and C_L are tuning circuit, and L_s effects on the gain, linearity and noise matching. The LNA features 2.5 dB noise figure at 1.57GHz, 18dB voltage gain, 250MHz bandwidth and S11 better than

12dB at the LNA passband. The LNA draws 2.5mA from a 1.8V supply yielding 4.5mW power consumption.

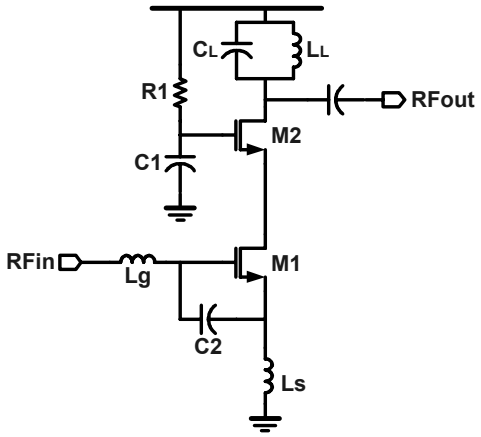


Fig. 4. A single-ended LNA.

The 1.57GHz RF signal is quadrature down-converted by the I-Q single balanced mixers, see Fig. 5, that are ac coupled to the LNA. Single-balanced mixers have lower input noise than the double-balanced mixers for the same power consumption. The problem of a single-balanced mixer is the leakage of LO frequency to the output. Since the LO frequency is much higher than the IF, the output LO frequency would be eliminated completely. The load is a simple resistor. The current consumption is 1.26mA for each mixer. The mixer gain is 16dB, and the LO rejection is -32dB.

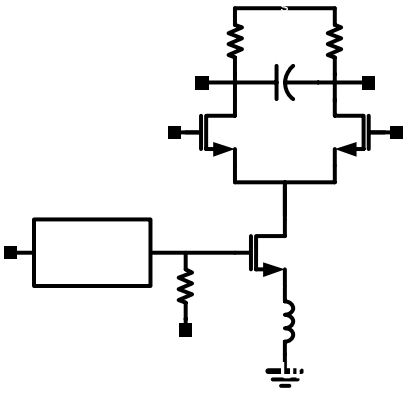


Fig. 5. A single-balanced mixer.

B. IF Section

The down-converted signal is amplified using an IF amplifier. A second-order integrated passive poly-phase filter, Fig. 6, has been used to recombine I and Q signal paths. Combination of I and Q signal paths in a single real path decreases the power consumption and the chip area. The poly-phase filter is an RC structure with inputs and outputs symmetrically disposed. A polyphase RC passive filter has zero power consumption, high image rejection, low sensitivity to mismatching in components, and high linearity. The average image noise rejection of the poly-phase filter is 20dB.

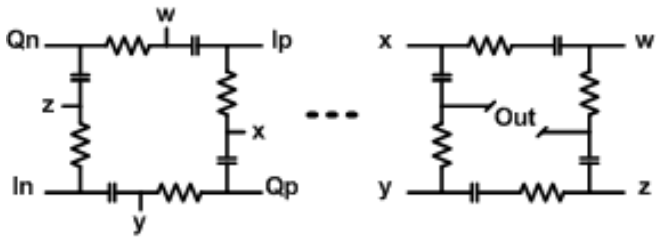


Fig. 6. A second-order poly-phase filter.

The IF-chain performs filtering and further amplification. An active RC filter is the best choice for its high linearity, high dynamic range, and variable gain. Although the filter noise is high, it has no effect on the receiver input noise due to the high gain of the LNA, mixer, and IF amplifier chain. A cascade of a bandpass and a low-pass filter is used to implement a fourth-order transfer function [2]. The programmable capacitor and the resistor banks control the gain in two filter stages without effecting the frequency response and bandwidth. The designed filter is centered a $4f_0$ (where f_0=1.023 MHz), and has a 5MHz bandwidth to cover the input signal spectrum over a wide range of temperature and process changes. The filter gain changes from -3dB to 52dB. The filtered signal is amplified by two IF amplifiers. The maximum gain of IF-chain is 86dB with a 55dB gain range. With 34 dB front-end gain, 120dB total on-chip gain is achieved. The quantizer quantizes the unsampled signal to a selectable level of 1, 1.5, or 2b. There is a source-follower output buffer to drive a 50 output load, with -2dB gain. The total IF strip drops 5.54mA from a 1.8V supply voltage.

IV. SYNTHESIZER

The quadrature LO signals generated for the receiver with a fully-integrated second order type-II phase locked loop (PLL) frequency synthesizer. It has a low phase noise fully-integrated quadrature LC VCO which uses 4nH square inductors with a Q of 6 and MOS varactors (Fig. 7). VCO frequency tuning range is about 400 MHz (considering process variation, temperature range between –40 to 125 degree, 10% variation on the L and C values). The minimum signal output amplitude of the VCO is about 0.2 Vp-p, because the mixer conversion gain drops in the smaller amplitude. The VCO output is divided by 128 and compared with the reference frequency after dividing by 2. Each divide-by-2 block consists of two master slave flip-flop implemented by CML logic with resistive loads. Each flip-flop is optimum for speed and power. The charge pump sends 0.3mA current pulses to the off-chip loop filter. The resulting voltage controls the VCO frequency. Table I, shows the synthesizer specifications.

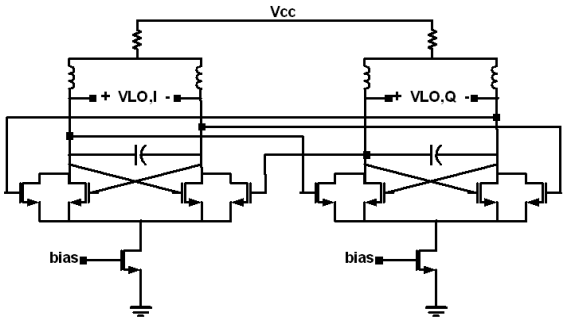


Fig. 7. A quadrature LC VCO.

TABLE I
THE SYNTHESIZER SPECIFICATIONS

Synthesizer:	
PLL Spurs	-60 dBc
Reference Frequency	12.276 MHz
Phase Noise @ 1 MHz	-105 dBc/Hz
Lock Time	< 10 μs
RMS Phase Error	6 degree
Current Consumption	6.5 mA

V. DESIGN FOR TESTABILITY

Trouble shooting methods are staggered wafers with extra devices, test structures, and design for testability. The staggered wafers with extra devices method needs to access to the circuit connections and the masks of the test structures method can not be used for production because the main circuit blocks are placed twice on the chip, one for full function and small pieces for testing. In the design for testability method some input and output drivers are considered to drive the input port and test the output port signal of the main circuit blocks. A number of working modes for the circuit are defined to check each block separately. A large number of controlling signals or a shift register with input programming signals, and logic circuits to produce the controlling signals are need.

Each circuit blocks could have a defect after fabrication due to insufficient modeling. Some test circuits are added for detecting the defective block and testing the other receiver blocks in the test structures method. Table II, shows all of the probable problems and the problem solving approaches for the receiver blocks.

The test circuits and internal test pins are added to the receiver as shown in grey colored sections of Fig. 3. The additional circuit only add %4 to the Si area. Critical to the success of this approach is shown in Fig. 8. By activating the buffer circuits, RF blocks can be tested in their original form and by making them high impedance normal operational mode is possible without disturbance. Additional test structures require many pins. A serial input digital block is used to minimize additional pins. Eight working modes were designed for the receiver, one for normal operating and the others for checking all of the circuit blocks (Table III).

TABLE II
ALL OF THE GPS RECEIVER PROBABLE PROBLEMS AND THE PROBLEM SOLVING (NOTE: MX ≈ MODE X)

Block	**Problem**	**Problem solving**
LNA	-Gain value wrong -Noise Figure is high -Input mismatch -Oscillates	-High gain: Reduce the input signal Level (m0) Low gain: Increase the input signal Level (m0) -Measure the NF at the IF output (m0) -Can be compensated by an external matching(m0) -Turn off the LNA input bias current, Increase the input signal level (m0)
Mixer	-I & Q mismatch -Low conversion gain	-Not critical (m0&6&7) -Change the mixer bias current (m0&6&7)
Polyphase	-RC error causes low image rejection -High loss	Measure the polyphase frequency response (image rejection & loss) by inputting I & Q signals to the polyphase and measuring its output signal (m4&5)
Filters	-Oscillation -Frequency response is out of spec, has peaking -Low noise rejection, high spurs	Measure the filters frequency response by inputting signal to it and measuring its output signal (m0&4)
Offset canceller	-Start up problem	-Check it at the IFamp3 output (m0&3)
Quantizer	-False threshold voltage levels	-Use an external quantizer from the IFAout output(m0)
VCO	-Output frequency is off -Does not oscillate -Low output amplitude	-Use external LO signal (m1&7) -Use external LO signal (m1&7) -Increase the VCO bias current (m0&2&6)
PLL Loop	-Does not lock	-Check divider, VCO, PFD separately (m2&6)
Divider	-Does not work	-Use external Lo signal, check the divider output(m6)
PFD	-Does not work	-Use of the PFD input signal, check the charge pump output (m5)
Charge pump	-Bias current changed	-Compensate it by changing the loop filter element values (m5)

TABLE III
EIGHT WORKING MODES FOR THE GPS RECEIVER (M0-7).

	Normal	Ext. VCO	VCO test	IF test	RC filter	PFD Poly Φ	Mixer VCO test	Mixer Ext. VCO
DPIQ	OFF	OFF	X	ON	X	ON	OFF	OFF
OMIQ	OFF	OFF	X	OFF	X	OFF	ON	ON
IFampA	ON	ON	X	OFF	X	OFF	OFF	OFF
PoSen	OFF	OFF	X	OFF	OFF	ON	X	X
FiltF	OFF	OFF	X	OFF	ON	OFF	X	X
IAampB	ON	ON	X	ON	OFF	OFF	X	X
IFAout	ON	ON	X	ON	ON	X	X	X
VCO	OFF	ON	OFF	ON	ON	ON	OFF	ON
DIV	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
DoSen	ON	OFF	OFF	X	X	ON	OFF	X
PFDF	OFF	ON	ON	X	X	OFF	ON	X

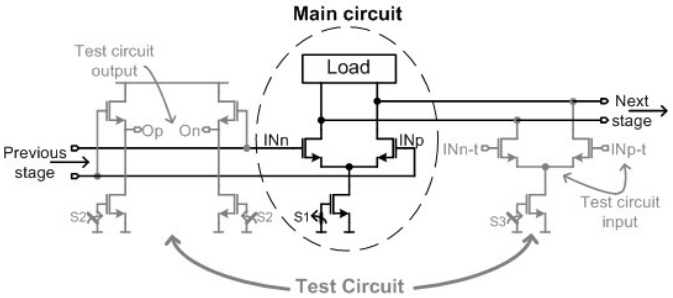


Fig 8. Test circuits for testing blocks.

All receiver blocks were tested separately after the first tape-out, using the defined working modes. All of the blocks specs except the VCO met the simulation results. The VCO oscillated at 1.9GHz. The RF-IF path and the divider block were tested with external LO frequency using m1 and m7 modes. The problem was solved in the next tape-out.

VI. MEASUREMENT RESULTS

The receiver is fabricated in a standard 0.18μm CMOS deep N-Well process. The chip specifications are summarized Table IV.

The IF filter frequency response and variable gain range is shown in Fig. 9. The pass-band ripple is less than 0.5dB. Figs. 10 show the 1,2-bit quantizer output. The GPS receiver has been housed in a standard 48-pin TQFP package that allowed multiple ground and test pins. A micrograph of the 6.5mm^2 IC is shown in Fig. 11.

TABLE IV
THE GPS RECEIVER SPECIFICATIONS

Receiver:	
Supply Voltage	1.8 volt
Technology	0.18 μm, CMOS
Architecture	Low IF
Input RF Frequency	1575.42 MHz, GPS L1
LO Frequency	1571.328 MHz
Input Matching	<-12dB (50Ω)
Noise Figure	3 dB
Total Voltage Gain	120 dB
VGA Range	-55 dB
Image Rejection	-20 dB
Output Format	1, 1.5 and 2 bit (F_{Sample}=4f_0 MHz)
Power Consumption	19.5 mA at 1.8 volt
Chip Area	6.5 mm^2

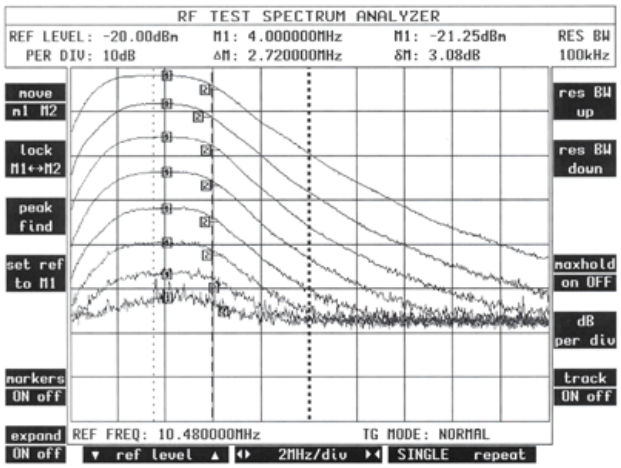
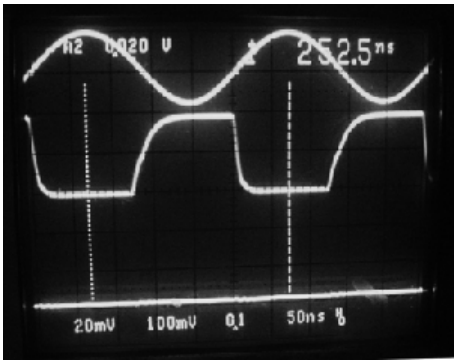


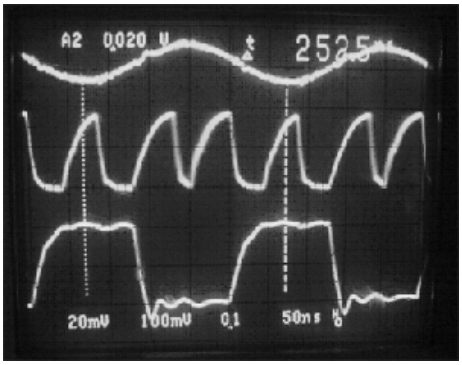
Fig 9. IF filter frequency response and variable gain range.

VII. Conclusion

A low-IF GPS radio was implemented in a 0.18μm CMOS process with a 19.5 mA power consumption in 6.5 mm^2. A serial input digital control with addition testing structure are used to the actual RF circuits in case of problems minimizing the number of Si runs.



(a)



(b)

Fig. 10. (a) 1-bit quantizer output, (b) 2-bit quantizer output.

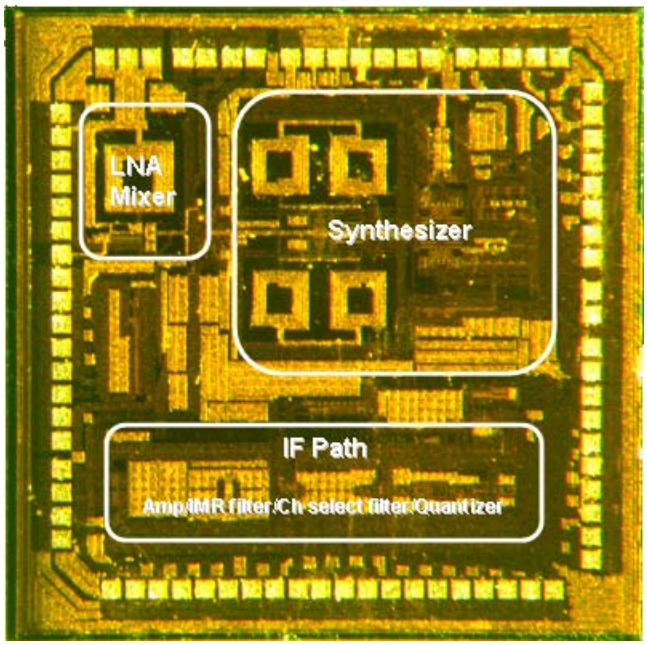


Fig 11. A micrograph of the GPS receiver.

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