Fast Flip-Chip Pin-Out Designation Respin by Pin-Block Design and Floorplanning for Package-Board Codesign

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Abstract— Deep submicron effects drive the complication in designing chips, as well as in package designs and communications between package and board. As a result, the iterative interface design has been a time-consuming process. This paper proposes a novel and efficient approach to designating pin-out for flip-chip BGA package when designing chipsets. The proposed approach can not only automate the assignment of more than 200 I/O pins on package, but also precisely evaluate package size which accommodates all pins with almost no void pin positions, as good as the one from manual design. Furthermore, the practical experience and techniques in designing such interface has been accounted for, including signal integrity, power delivery and routability. This efficient pin-out designation and package size estimation by pin-block design and floorplanning provides much faster turn around time, thus enormous improvement in meeting design schedule. The results on two real cases show that our methodology is effective in achieving almost the same dimensions in package size, compared with manual design in weeks, while simultaneously considering critical issues in package-board codesign. To the best of our knowledge, this is the first attempt in solving flip-chip pin-out placement problem in package-board codesign.

I. Introduction

Because of deep submicron (DSM) technology, chips now contain more functionality and are being driven to higher performance levels than ever before. Consequently, with more functionality on the chip, designers have to deal with higher I/O densities, more signals coming out of a chip and tigher geometries [7]. This leads to the complication in designing package which accommodates chips, as well as the board which accommodates the packages. As a result, the ability to design the chip, the package and surrounding system concurrently becomes a primary advantage, but also a chanllenge.

Recently chip-package codesign has drawn attention under these circumstances, for example [2], [11]. However package-board codesign, which is definitely not a trivial work, still needs more works, especially under DSM effects. There were several works [4], [12], [3], [8] which are related to package and printed circuit board (PCB) physical designs. [4] presented a style for ball grid array (BGA) ball-out, but shielding pins used for preventing pin-to-pin crosstalk were not considered. Moreover, when they try to keep the package cost small, this style puts a restriction on the maximum package size. Thus, there will be a limit to the number of BGA balls that can be used for power delivery, and area for power delivery from motherboard to package. [12] proposed an algorithm which assigned and routed the solder bumps of a BGA package to a set of fanout points in a single layer. However this work only created a topological routing, not precise geometry layout, and only the routability issue on PCB is considered. [3] presented a simulated annealing algorithm to find a pin assignment solution which considered the routability issue on PGA package and PCB, but no other DSM effects were considered.

Fig. 1(a) shows the typical interface design flow for IC-package-PCB codesign. In general, IC designers finish the pin designation based on experience (rule-of-thumb). In order to tradeoff signal performance and package cost, they always take a few weeks to modify package size, rework package substrate and PCB layout, and rearrange pin-out. This conventional process can not efficiently estimate an accurate package size during designating pins for flip-chip BGA and possibly degrade signal performance due to the weakness on product experience and basic design concept. Furthermore, these costly rework constantly postpone the schedule of chip implementation, thus lengthen the time to market (TTM). Hence this paper presents a novel approach of designating pin-out to replace heavy-loaded human design by automation process which accounts for practical experience and techniques. Fig. 1(b) illustrates the proposed approach. Obviously this approach will significantly shorten the runtime throughout the automation process. It can not only automate pin-out designation efficiently, but also optimize package size during design stage, thus reduce the time of iteration.

The contributions presented in this paper are as follows:

- We have designed six signal-pin patterns for pin block construction in package design. Signal integrity, power delivery, and routability have been accounted for in those patterns. This helps to speed up the process of pin-out designation.
- We have proposed a near optimal approach to minimize package size by mathematical (linear) programming formulation.
- We automate this pin-out designation process for package-board codesign. The experimetal results show that our solution can achieve almost the same results as manually designed by experienced designers, with much less time.

The remainder of the paper is organized as follows. Section II discusses the flip-chip BGA package design with PCB and DSM effects consideration, while Section III describes our pin-out designation by near optimal planning in package size. Section IV shows the experimental results followed by the conclusion in Section V.

II. Pin-out Designation by Considering Signal Integrity and Power Delivery in Package-Board Codesign

Fig. 2 depicts a sketch of PCB layout. Usually PCB board contains several kinds of components and connectors which are applied to specific interfaces. The length of signal net from package pin to component or connector on PCB is the primary contributor

This work was partially supported by the National Science Council of Taiwan ROC under grant No. NSC 95-2220-E-009-028.

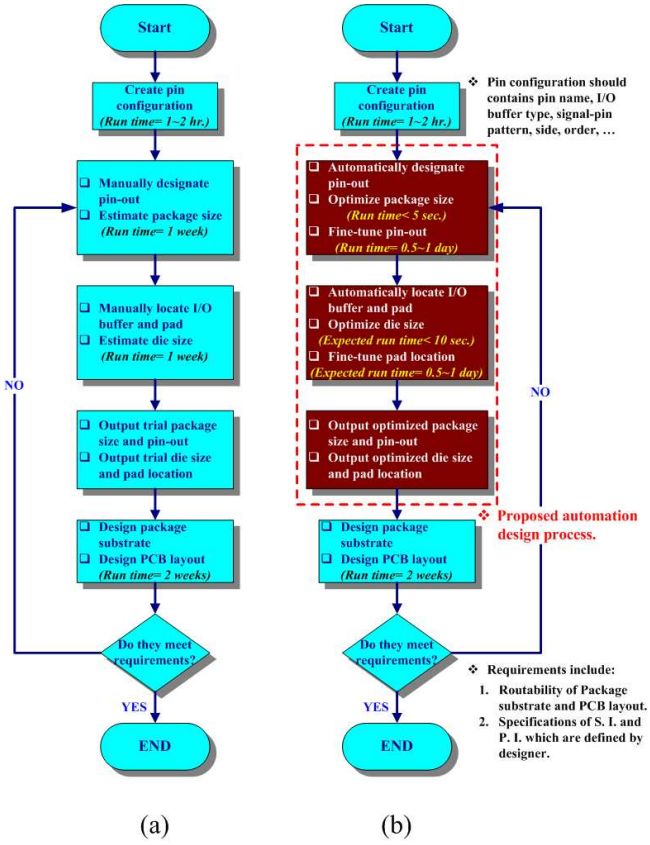

Fig. 1. The typical flow and proposed approach in interface design for IC-package-board codesign. The focus of this paper is to automate pin-out designation and to minimize package size during design stage.

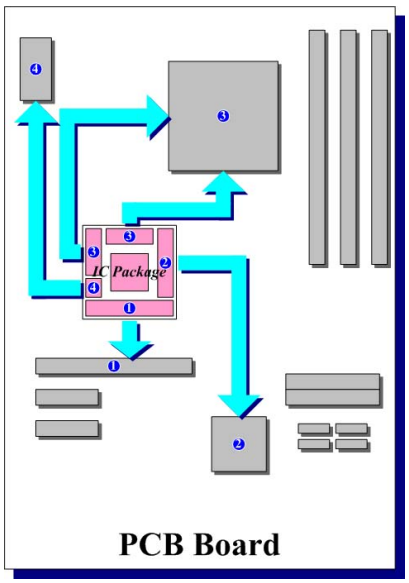

Fig. 2. A general layout of PCB board. The location of pins on IC package should be restricted in specific regions to meet minimum net-length.

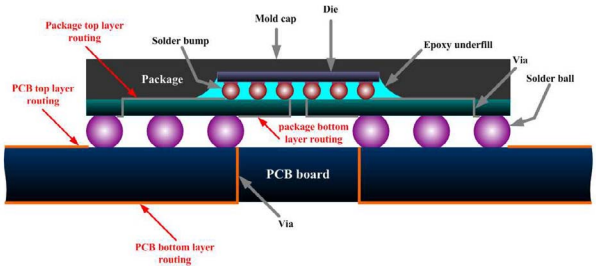

Fig. 3. Simplified cross-section of a flip-chip package which is mounted on PCB board.

to parasitic inductance. Therefore, package pins will exacerbate simultaneous switching noise (SSN) by increasing the parasitic inductance in the signal nets [6]. In order to minimize the physical length of the package pins thus reduce the total parasitic inductance, the signal pins should be allocated and restricted in particular region according to the certain location of corresponding components or connectors. Fig. 3 shows the simplified cross-section of a flip-chip package which is mounted on PCB board. Based on experienced method, the bumps which are beneath the die, located close to die edge will be routed signal nets through package top layer. On the contrary, the bumps located around the core of die will be routed signals through vias and fanned out nets on package bottom layer. For package pins, which are solder balls, the connected signal nets are acted according to the same rule to share finite routing resource.

Another crucial factor of successful pin designation is routability. For routing issue, it should be noted that the net width and spacing on PCB are the critical constraints. The excess row number used for placing signal pins will undoubtedly cause routing congestion due to restricted area between pins. Fig. 4 demonstrates the routing pattern on PCB top layer and package bottom layer respectively. For instance, when the diameter of PCB pad is 14mil (1 mil = 25.4 um), pad pitch is 1000 um, signal net width is 5mil and net spacing is 5mil on 4 layer PCB board, the space between two pads can only be penetrated by two nets. That means only three rows of signal pins can be fanned out nets on PCB top layer. Hence the maximum row number of outer pins is nine and that of signal pins is seven (exclusively happened in corners of the package). Fig. 5 lists the restricted row number of signal pins in different package size.

As for signal integrity, return path inductance should be considered as well. The unfavorable placement and number of return path pin, power or ground, will maximize current return loops and increase return path inductance [6]. This will dramatically degrade signal integrity and exacerbate radiated emissions. The optimal pin designation is to place signal pin and power or ground pin proximally close to each other, so that each signal pin can be tightly coupled to a return path pin. This will minimize the effect of the return path inductance. In [5], [10], [9], the effects of shielding, return path and reference plane are considered in package and PCB designs. However, the optimal design, in terms of signal integrity concern, will create such signal-pin blocks which have fewer signal pins within a large block area.

Fig. 6 illustrates six proposed options of signal-pin pattern for laying nets out on four layer PCB board. There exists tradeoff between signal performance and package cost. The first signal-pin pattern exhibits each pair of differential signal which has been surrounded by ground pins. These ground pins can be performed as adjacent return path pins to minimize total inductance and as shielding pins to isolate pin-to-pin crosstalk noise. Moreover, the

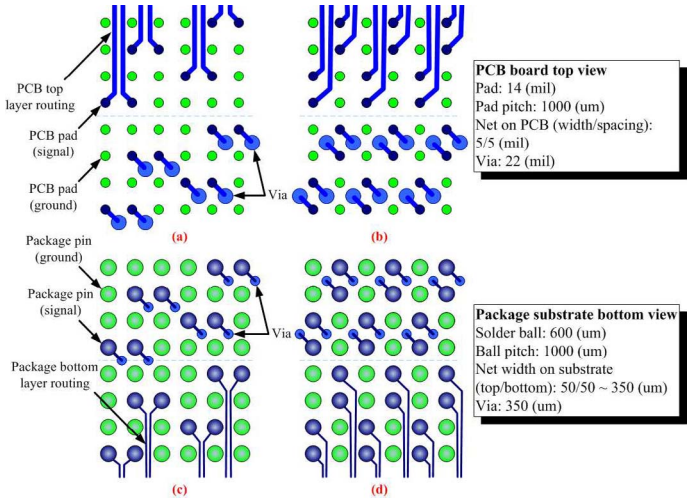

Fig. 4. The routing pattern on PCB top layer (a)(b) and package bottom layer (c)(d).

Package size (mm) (Width x Height)	Pin number (Row x Column)	Row number of outer-pin (power-pin, ground-pin and signal-pin)		Row number of outer-pin (signal-pin only)	
		Max.	Avg.	Max.	Avg.
37.5 x 37.5	36 x 36	9	8	7	6
35 x 35	34 x 34	9	8	7	6
31 x 31	30 x 30	9	8	7	6
27 x 27	26 x 26	9	8	7	6
...	...	9	8	7	6

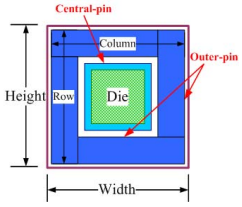

Fig. 5. The row number of signal-pin with different package size (PCB pad=14 mil, pad pitch=1.0 mm, net width=5 mil, net spacing = 5 mil, for four layer PCB board).

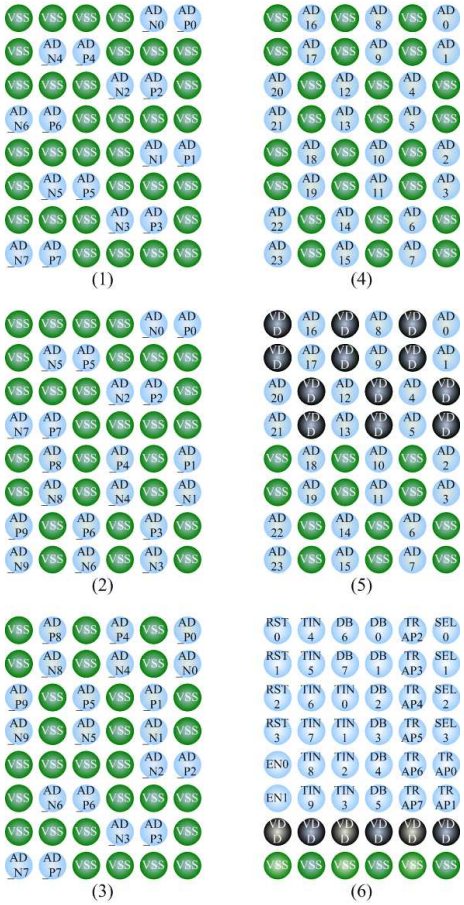

Fig. 6. Six pin patterns presented in this paper. There exists tradeoff between routability and signal integrity concerns. The first pin pattern has better signal integrity, while the sixth one has the most efficient pin designation. In those patterns, AD_P0/AD_N0 is for differential signal (high speed), AD is for single-ended signal (high speed), and SEL or TRAP in sixth pattern is for single-ended signal (low speed or long-pause signal).

primary concern of differential system is on impendence-matching of nets. The first pattern has an exclusive advantage of balancing nets on PCB as well as package substrate layout, shown in Fig. 4(a) and (c), thus it is optimal for differential signals, from the performance perspective. The only disadvantage of this pattern is poor pin designation efficiency. In most cases, if the return current flows on the ground planes, the signal pins should be coupled to the ground pins or vice versa. Furthermore, each signal pin should be coupled to both one power and one ground pin. If a signal is coupled to just one power pin or just one ground pin, this case will emerge based on signal type and its configuration. The fourth and fifth signal-pin patterns provide two options for specific bus. The fifth pattern has better power delivery characteristic than the fourth one because of locating power pins. These two patterns arrange pins more efficiently than first pattern, but they both have worse signal integrity on PCB top-layer-routing and package bottom-layer-routing due to poor impedance-matching, shown in Fig. 4(b) and (d). As compared with above-mentioned patterns, the second and third patterns are the compromises between signal performance and package cost. The sixth signal-pin pattern is the most efficient pin designation among all patterns since it contains most signal pins than other patterns. The major disadvantage of this pattern is that it ignores all signal integrity concerns and can only be applied to test-in, test-out or long-pulse control signal, which has less sensitivity in crosstalk.

According to the product experience and basic concept of signal integrity, we have proposed six patterns and characterized them in Fig. 7. Designers can easily choose a specific pattern along the specification of individual bus, or designers can design pin patterns for their specific purposes. Our automation program can compatible to other well-defined patterns which has sensible efficiency, routability and signal integrity.

Considering power delivery issue, this paper brings up an idea of establishing a power-pin block. According to the power analysis result and production experience, designers can freely define the demand of power pins for individual signal configuration. While the signal-pin block is constructed, the proposed automation process will create power-pin block then place it adjacent to the related signal-pin block shown in Fig. 8.

III. Pin-Out Designation Automation by Pin-Block Construction and Floorplanning

A. Pin-Block Construction

First, designers determine pin configuration chart based on experience about the location of component on PCB and the characteristics

	Application	Signal-pin NO.	Pin-to-pin crosstalk immunity	Net balance				Signal shielding on package substrate (Power/Ground)		Power delivery aware	Pin-designation efficiency
				PCB board		Package substrate					
				Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer		
Pattern (1)	Differential signal	16	Excellent	Good	Good	Good	Good	Ground	Ground	Without	Not good
Pattern (2)	Differential signal / Single-ended signal	20	Good	Good	Good	Good	Not good	Ground	Ground	Without	Average
Pattern (3)	Differential signal / Single-ended signal	20	Good	Not good	Good	Good	Good	Ground	Ground	Without	Average
Pattern (4)	Differential signal / Single-ended signal	24	Excellent	Not good	Good	Good	Not good	Ground	Ground	Without	Good
Pattern (5)	Differential signal / Single-ended signal	24	Excellent	Not good	Good	Good	Not good	Power	Ground	With	Good
Pattern (6)	Single-ended signal	36	Not good	Not good	Not good	Not good	Not good	None	None	With	Excellent

Fig. 7. Characteristics of signal-pin patterns. According to the properties and requirements of specific signal, we can select a proper pattern for designating pins.

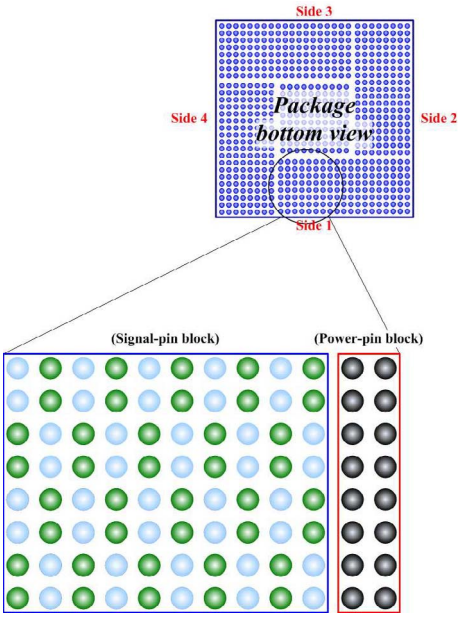

Fig. 8. A complete pin block includes signal-pin block and its related power-pin block. It is located on the region close to corresponding component on PCB.

Signal-pin name	I/O buffer type	I/O width (um)	I/O height (um)	Selected signal-pin pattern	Group	Side	Order	Power-pin name	Power-pin NO.
AD_P[0:7]	AIO1XH0J	40	500	1	1	1	1	VDDA	10
AD_N[0:7]	AIO1XH0J	40	500	1	1	1	1	VDDA	10
…	…	…	…	…	…	…	…	…	…
AD[0:15]	BIO1XH0J	30	350	3	2	1	2	VDDB	8
…	…	…	…	…	…	…	…	…	…
TEST_IN[0:6]	CIO1XH0J	25	400	4	3	2	1	VDDC	5
TEST_OUT[0:6]	CIO1XH0J	25	400	4	3	2	1	VDDC	5
TRAP[0:6]	CIO1XH1J	25	400	4	3	2	1	VDDC	5
…	…	…	…	…	…	…	…	…	…

Fig. 9. An example of pin configuration chart. In this pin configuration we can define specific information as inputs of our proposed automated approach.

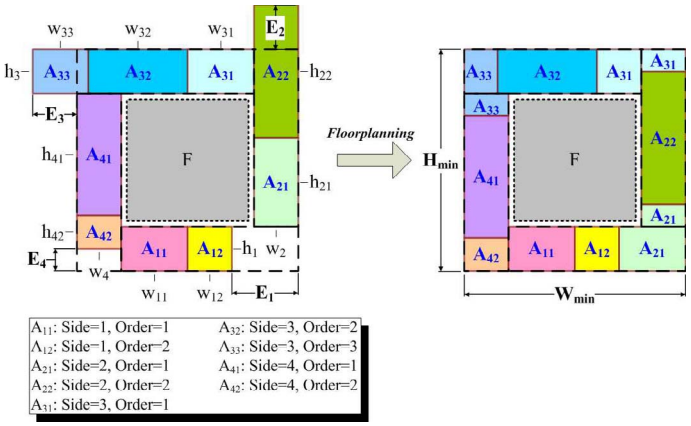

Fig. 10. A minimum package size can be obtained after we designate and floorplan all pin blocks.

of each signal group, an example is shown in Fig. 9. In general, it always needs 1 or 2 hours to define the pin configuration for high pin-count chip. From previous discussion, signal integrity, power delivery and routability issues should have been accounted for when signal pins are placed. The pin configuration must include all critical parameters defined for placing signal pins, including the distribution region (side), placement sequence (order), selected signal-pin pattern and the number of power pins. Then both signal-pin block and power-pin block will be built and further grouped into one block A_{ij} for specific bus, where i and j are to represent side and order that blocks are located on and defined in pin configuration by designer. Furthermore designer can acquire parameters w_{ij} and h_{ij} (w and h represent the width and height of each block respectively).

After finishing the implementation and placement of all blocks, a rough pin designation will be obtained, shown in Fig. 10. At the same time, parameters E1 to E4 can be evaluated from this rough pin designation (E1 to E4 represent the width or height of the empty and excess area in each side of minimum package model).

B. Minimizing Package Size and Finalizing Pin-out Designation by Pin-Block Floorplanning

The next step is to optimize package size and acquire a feasible pin designation. The following are objective function and constraints, formulated as a linear program. We use an open domain solver to obtain minimize package size:

Minimize

$$f = \sum_{j=1,3}(\sum_i w_{ji} + E_j)h_j + \sum_{j=2,4}(\sum_i h_{ji} + E_j)w_j + F$$

subject to

$$W = w_4 + \sum_i w_{1i} + E_1 = w_2 + \sum_i w_{3i} + E_3 \quad (1)$$

$$H = h_1 + \sum_i h_{2i} + E_2 = h_3 + \sum_i h_{4i} + E_4 \quad (2)$$

$$W = H \quad (3)$$

$$E_1 + E_2 + E_3 + E_4 \geq 0 \quad (4)$$

$$F \geq c \quad (5)$$

TABLE I
TWO INDUSTRIAL BENCHMARKS USED IN THIS PAPER.

	Signal bus	Pin num	Group	Selected signal-pin pattern	Side	Order	Power-pin number
Case 1	Bus#1	66	1	2	1	1	32
	Bus#2	27	2	3	2	1	8
	Bus#3	37	3	4	2	2	24
	Bus#4	39	4	1	3	1	N/A
	Bus#5	42	5	1	4	1	24
	Bus#6	58	6	4	4	2	24
Case 2	Bus#1	66	1	2	1	1	24
	Bus#2	27	2	3	2	1	8
	Bus#3	95	3	2	2	2	N/A
	Bus#4	100	4	2	3	1	8
	Bus#5	42	5	4	4	1	16
	Bus#6	16	6	4	4	2	7

where w_{1i},h_1,h_{2i},w_2,w_{3i},h_3,h_{4i},w_4 can be evaluated in the previous step, all shown in Fig. 10. F is the center area of BGA package. In principal, the power and ground pins are located at the center of package and the die is located upon these power and ground pins. As a result, the heat generated from the die can be transferred out through these pins [1]. Thus increasing more power and ground pins located at the center area will improve heat dissipation but enlarge the value of F, thereby enlarge the package size. We use (5) to define the value of F in accordance with physical die size, where c is user specified parameter. Use (1) to (3) will restrict the shape of package to be square. The purpose of (4) is to insure that the minimum package size can accommodate all pin blocks with almost no void pin positions.

After E_1 to E_4 are obtained, we can easily recognize the position of the empty and excess area in the minimum package. The final step of proposed methodology is to floorplan pin blocks, which are to shift the location of pins in the excess area and fill them into the adjacent empty area. It can completely eliminate exceed area and keep those pins being located around the particular region restricted in previous step. Fig. 10 shows an example, where there are two excess areas occurred in second and third side (upper right and upper left corners) and two empty areas occurred in first and fourth side (bottom right and bottom left corners). Some of the pins in the excess areas will be shifted into the empty areas through a simple procedure, then acquire an optimized package size, and we finish the pin designation process.

IV. EXPERIMENTAL RESULTS

We have implemented our methodology in C++ and the platform is on AMD Sempron 1.75GHz with 1GB memory. We use two industrial chipset cases as our benchmarks, shown in Table I, which comes from the pin configuration charts (Fig. 9). Table I, Fig. 11 and Fig. 12 show the results of pin-out designation for these two benchmarks. Based on Table II which is obtained from linear programming formulation shown in Section III.B, we can get corresponding parameters to floorplan all pin-blocks. The runtime of designating pin-out is less than 5 second for both cases. For Case 1, our pin-out designation (Fig. 11(b)) is perfectly matched with manual design (Fig. 11(c)) achieved by an experienced engineer, which spent long turn-around time to respin the design (usually weeks). For Case 2, due to more pin numbers in some buses and signal-pin block pattern usage (while pin number is not divisible by 8 will generate void position), a slightly larger package size (Fig. 12(e)) is achieved, but still very close to the manual design (Fig. 12(f)).

TABLE II
THE EXPERIMENTAL RESULTS OF CASE 1 AND CASE 2.

	E_1	E_2	E_3	E_4	$\sum_i E_i$	Central p/g pins (F=rowxcol)	Eval min package (WxH)
Case 1	-3	2	8	-7	0	10x10	26x26
Case 2	3	-9	-3	12	3	14x14	31x31

V. CONCLUSION

We have proposed in this paper a novel and efficient approach in pin-out designation automation in flip-chip BGA packaging for package-board codesign. Due to tradeoff in signal performance and package cost, conventional approach usually take weeks to modify package size and rework package substrate and PCB layout, and rearrange pin-out. The proposed approach can be replaced by our efficient methodology. By considering signal integrity, power delivery, and routability in pin-out block design, our framework provides good signal quality while achieving close-to-minimum package size, which reduces package cost.

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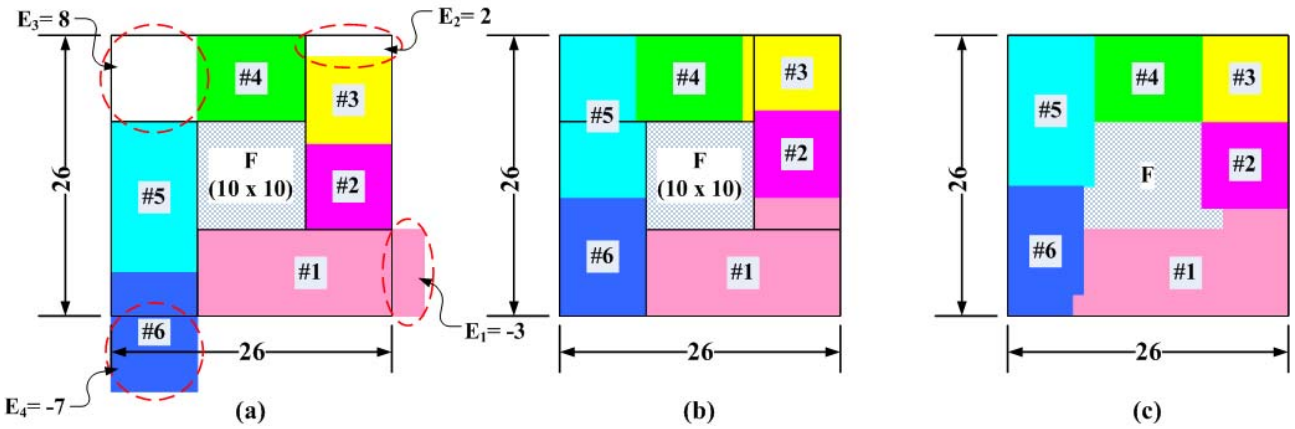

Fig. 11. Experimental results of case 1: (a) Placement of blocks in minimum package evaluation. (b) Sketch of pin-out after floorplanning.(c) Manually designated pin-out. Our approach can produce the same dimensions as in manual design.

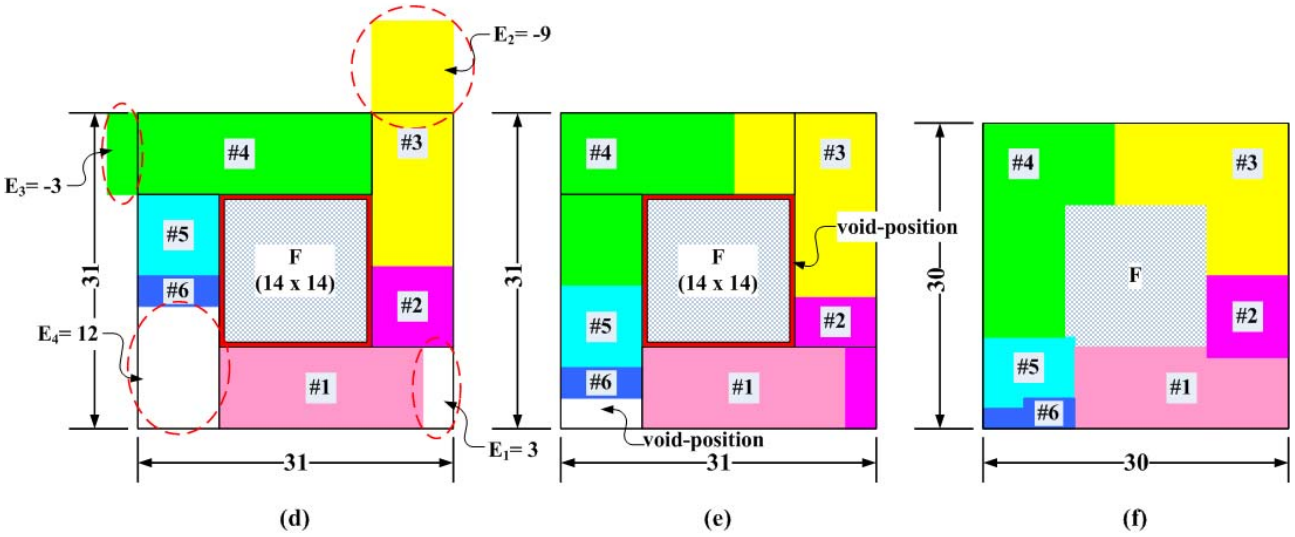

Fig. 12. Experimental results of case 2: (d) Placement of blocks in minimum package evaluation. (e) Sketch of pin-out after floorplanning. (f) Manually designated pin-out. Our approach can produce a pin designation layout (31x31) very close to the manual one (30x30).