Fast and Accurate OPC for Standard-Cell Layouts *

David M. Pawlowski, Liang Deng, Martin D. F. Wong
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign
{dmpawlow,ldeng,mdfwong}@uiuc.edu

Abstract— Model based optical proximity correction (OPC) has become necessary at 90nm technology node and beyond. Cellwise OPC is an attractive technique to reduce the mask data size as well as the prohibitive runtime of full-chip OPC. As feature dimensions have gotten smaller, the radius of influence for edge features has extended further into neighboring cells such that it is no longer sufficient to perform cellwise OPC independent of neighboring cells, especially for the critical layers. The methodology described in this work accounts for features in neighboring cells and allows a cellwise approach to be applied to cells with a printed gate length of 45nm with the projection that it can also be applied to future technology nodes. OPC-ready cells are generated at library creation (independent of placement) using a boundary-based technique. Each cell has a tractable number of OPC-ready versions due to an intelligent characterization of standard cell layout features. Total number of cells with boundaries in the OPC-ready library only increases linearly with the number of cells in the original library. Results are very promising: the average edge placement error (EPE) for all metal1 features in 100 layouts is 0.731nm which is less than 1% of metal1 width, creating similar levels of lithographic accuracy while obviating any of the drawbacks inherent in layout specific full-chip model-based OPC. For even small circuits, there were runtime reductions of up to 100X and a potential 35X decrease in mask data size.

I. Introduction

Lithography continues to be the backbone of circuit fabrication. The use of sub-wavelength lithography is needed to continue the progression of technology nodes. To adapt to the optical degradation that becomes exaggerated in the sub-wavelength regime, various reticle enhancement techniques (RET) are employed in mask development. One of the most prominent types of RET is optical proximity correction (OPC). Two broad categories of OPC exist, ruled based and model based. As IC technology advances, the need for more aggressive correction demands the accuracy of model-based OPC. There are drawbacks, however, to using model based OPC. The first is the large storage requirement for mask data due to the need of more numerous and complex geometries representing the correction. A second problem is the large number of computation hours (e.g., days of OPC computations on computers running in parallel). This problem will only get worse as the increases in circuit imaging complexity outpace the increase in computation capacity. Another drawback is that the simulation models, although increasingly complex, do not account for all possible sources of printing variation. This can result in actual feature printing to deviate from what the model described, potentially causing imaging failures resulting in yield loss.

With hierarchical structure, an OPC-ready standard cell library will not only have huge runtime saving and much less data size, but also give a more predictive performance of the design. A Cellwise OPC methodology was proposed in [1] for 90nm node. The environment for poly and contact layers outside cells is reproduced by dummy features. This proposed method leads to very small errors (most within 6%), compared to full-chip OPC. The mask data size and runtime are both reduced dramatically. However, as features are placed closer, one dummy feature may not be sufficient to simulate the environment. One Solution was proposed in [2]. It divides the cells into core parts and boundary parts. The OPC solutions for core parts are determined by its boundary counterparts before placement. The boundaries accept full-chip OPC after all cells are placed. Although this method can be implemented for 65nm node and beyond, the mask data size was only reduced to 40%. Best case runtime speeds up 5.5X for a large design. Some of the benefits of cellwise OPC are lost due to the involvement of full-chip flavor OPC. Library cells are not OPC-ready because of the rip-off of boundaries, which makes their characteristics are less predictive.

This work describes a design methodology that ameliorates these problems for standard cell design beyond 90nm node. The core of the method is developed around two of the main principles guiding OPC. The first is that resultant OPC edges are uniquely determined by the target geometry's size and the size and proximity of neighboring geometries. The second principle is that the radius of influence (ROI), the range of distance in which features have a non-negligible effect on one another, is approximately 600nm for a 193nm wavelength illumination source. Features outside this distance can be effectively ignored. Due to the nature of standard cell design, there are a discrete number of potential geometric patterns represented in any given layout. By limiting the potential boundary features of standard cells, the number of potential patterns becomes manageable. The OPC corrected edges can be accurately determined before layout on a per cell basis for a given cell library, removing design specific simulation and subsequent full-chip OPC correction.

In the next Section, factors that enable our proposed method are discussed. Details of boundary-based cellwise OPC are

*This work was partially supported by the National Science Foundation under grant CCR-0306244

1-4244-0630-7/07/$20.00 ©2007 IEEE.

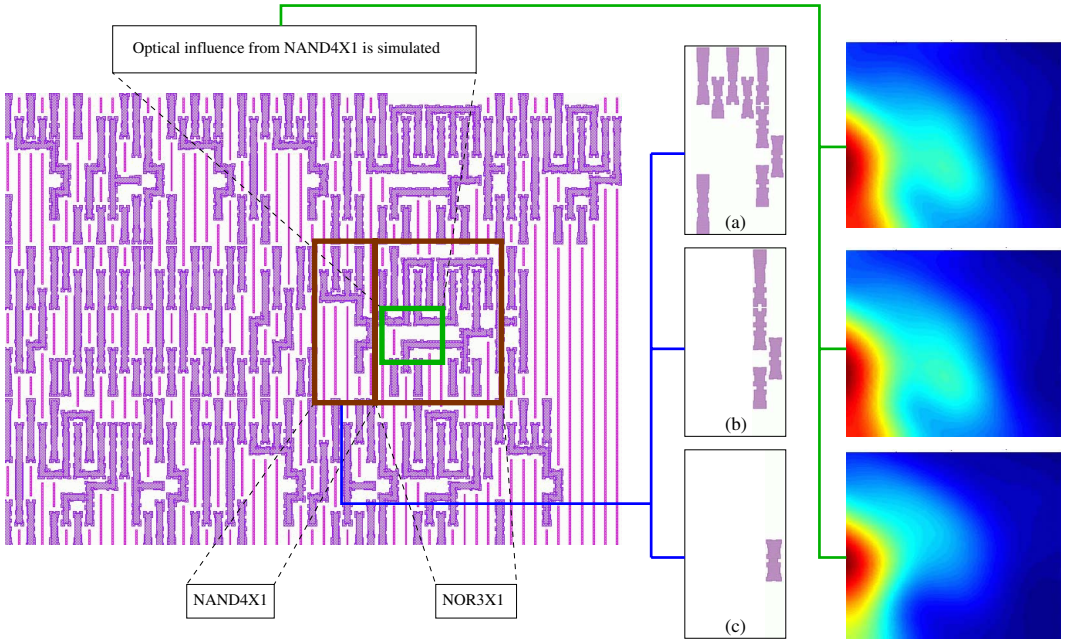


Fig. 1. In this layout, two marked cells are adjacent. Only metal1 layer is shown. The OPC solution for NOR3X1 is affected by NAND4X1. We simulated the aerial image from features of NAND4X1 in the NOR3X1 cell. (a) All features in NAND4X1 are considered in simulation. (b) In our boundary-based cellwise OPC method, limited features are needed to reproduce the optical influence from NAND4X1. (c) Less boundary features could lead to large error. If only one column is used as boundary, it cannot simulate the environment for NOR3X1 correctly.

shown in Section 3. Results are presented and analyzed in Section 4. We will conclude this work in Section 5.

II. Basic Idea

The size and proximity of neighboring features uniquely determine the OPC edges of a feature that enable more accurate printing. Using a 193nm illumination source, neighboring features are classified as features within the 600nm ROI [1]. This presents an interesting situation for standard cell design. If a feature is near the center of the cell, its ROI may lie completely within the cell. Because the layout within the boundaries of the standard cell is known, the corresponding OPC edge manipulations for these center features are independent of full-chip layout and can be predetermined. However, if a feature is near the cell edge, its ROI can extend beyond the borders of the cell. Features from neighboring cells can potentially lie within this region resulting in a layout specific OPC solution for edge features.

As dimensions have gotten smaller, the radius of influence for edge features has extended further into neighboring cells such that it is no longer sufficient past the 90nm technology node to perform cellwise OPC independent of neighboring cells. The methodology described in this work accounts for features in neighboring cells and allows a cellwise approach to be applied to cells with printed gate lengths of 45nm with the projection that it can also be applied to future technology nodes.

Throughout the rest of this paper metal 1 is used as the representative layer. There are many characteristics of metal 1 that enable it to sufficiently prove the feasibility of the boundary-based cellwise method. The first is the pervasiveness of metal 1 in the cell library. It is present in every cell in a wide range of patterns, allowing a thorough testing of the methods adaptability to a wide range of layouts. Metal 1 is also found close to cell edges, creating a high degree of interaction between features in different cells. The final reason is its relatively narrow pitch. Our goal was to demonstrate the feasibility of this method using printed gate lengths of 45nm. To achieve this we roughly followed the standards suggested in the ITRS roadmap for the 70nm DRAM half-pitch. The other potential layer choice is poly, primarily due to its small feature size. The feasibility of using both layers was examined and it was determined that the additional interaction due to the proximity of metal 1 to cell edges outweighed the effects of the smaller poly dimensions. This suggested a more pronounced interaction of features in different cells on metal 1 than on poly. Metal 1 was thus determined to be the most relevant layer on which to perform testing.

To enable the boundary-based cell-wise design, there are several constraints that must be applied to the standard cell library. The first restriction is the enforcement of a fixed pitch in both the horizontal and vertical directions. Pitch is defined as the space between the centers of similarly oriented features. Due to off-axis illumination (OAI), and various optical characteristics, a lithography process is tuned to a range of allowable pitches. As lithography systems get pushed to their resolution limits, the process window becomes narrower. Extending this to our considered technology node, a fixed pitch is not overly restrictive [3]. It allows considerable efficiency in the design methodology at a relatively low cost in layout flexibility.

To further reduce the number of potential boundary patterns only vertically oriented features are considered to have appreciable effect. Taking only vertical features into account is prac-

tical due to the relative importance of optical influence between parallel features as opposed to perpendicular features. In our experiments, we considered interactions between cells to be limited to adjacent cells on the same row. Therefore, parallel feature interaction is limited to the vertically oriented features. Features oriented in the same direction have greater influence because of the optics involved off-axis illumination. They also have greater influence because two parallel features are on average closer to each other than perpendicular features of equivalent minimum spacing.

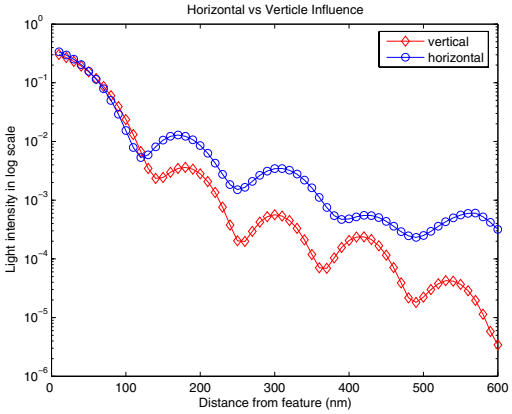


Fig. 2. The influence outside a feature of corrected by OPC. Light intensity are measured in 600nm region start from its original edges.

Moreover, the ROI is a result from partial coherent light source. Theoretical ROI value [4] for small features can be found by Equation 1.

$$R = \frac{1.12}{\sigma}\frac{\lambda}{NA} \tag{1}$$

where λ is the wavelength, NA is the numerical aperture, and σ is the partial coherent factor. ($\sigma = 0$ corresponds to the coherent case, and $\sigma = \infty$ corresponds to incoherent case.) A typical quasar light source, which we used in our experiments, has an equivalent partial factor $\sigma = 0.4$. It yields a 570nm ROI for experimental setting. However, this ROI is only meaningful for small openings on mask. If the feature is large, the influence diminishes quickly outside the feature. We compare the light intensity outside the feature on both horizontal and vertical directions in Figure 2. The vertical influence is one magnitude less than the horizontal one at the same distance. This further validates our approach to consider the vertical lines only. Figure 3 shows the experiment results on vertical influence. The OPC correction of a cell was performed in an isolated environment. The cell with corrected features was then duplicated and placed in a position equivalent to being on an adjacent row. Edge placement error (EPE) is used to measure the OPC quality [5]. The top cell was shifted relative to the bottom one and the average EPE was calculated at each point. Negligible effect is noted when comparing EPE. This conclusion was also verified by the overall results presented later in Section 4.

With only vertical features and fixed pitch considered, an ROI region can be divided into columns. Each column has a width equivalent to the pitch. Using our considered pitch

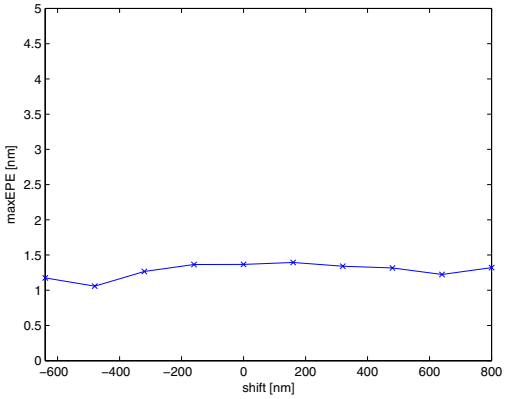


Fig. 3. Average EPE of bottom cell of two stacked bufx1 cells as top instantiation is shifted.

every column has four columns on each side within its ROI. Translating this to interactions between cells, a feature on the cell boundary can theoretically influence four columns into the neighboring cell. The amount of influence these columns have on features in the neighboring cell is determined by their distance from the cell border. This is true because although the radius of influence extends to 600nm, a mask feature that is 300nm away will have a decidedly greater influence than a feature that is 500nm away. Experimentally it is determined that the influence of the third and forth columns are limited, and their effect on the neighboring cell can be ignored as shown in Figure 1 . Testing also indicates that the second column has minor influence. The main influence of the second column on the neighboring cell is seen indirectly. The presence of a feature in the second column influences the correction of features in the first column which in turn affects the neighboring cell. The majority of the optical effects that the second column contributes to features in neighboring cells can be modeled by considering the column full or empty based on the percentage of the column that is occupied by mask features. This allows unrestricted feature layout in the second column without increasing the effective number of potential boundaries seen by neighboring cells. Features in the first column, however, are subject to rigid constraints. They have considerable influence on the features in neighboring cells and their precise dimensions are therefore restricted. This is done by limiting the features in the first column to a set of potential geometries.

To determine the set of potential geometries that can occupy the first column another important simplification in feature interaction is utilized. This simplification is allowed due to the general layout topology of standard cells in which PMOS gates are found in one half of the cell and NMOS gates are found in the other half of the cell. In this topology many features exist completely on either the top or bottom allowing the cell to be split into two sub-cells. This reduces the number of potential feature layout patterns in the edge regions that can influence features in neighboring cells. The reduction is due to the previously stated optical importance of features oriented in the same direction. The importance of parallel feature interaction allows the neighboring cell optical environment of features in

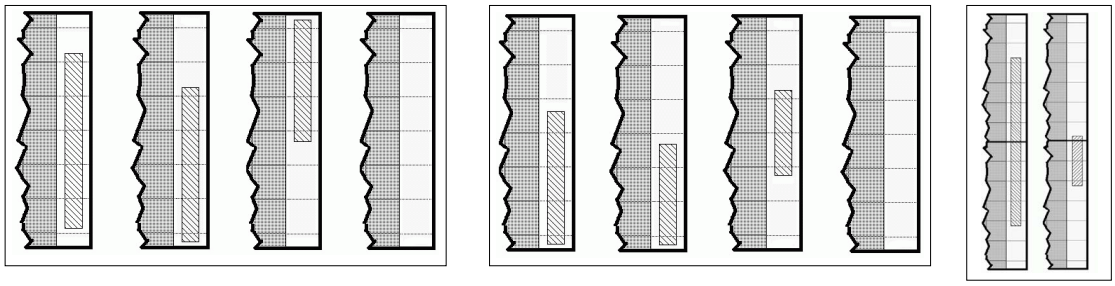


Fig. 4. Set of allowable first column features for top and bottom sub-cell. Some allowable first column features cross sub-cells. Shown for right boundary, however same set used for left boundary.

the top or bottom sub-cell to be determined solely by features in the corresponding neighbor top or bottom sub-cell. Considering all these restrictions and modifications, we will detail the boundary-based cellwise OPC library design in the next section.

III. Boundary-based Cellwise OPC

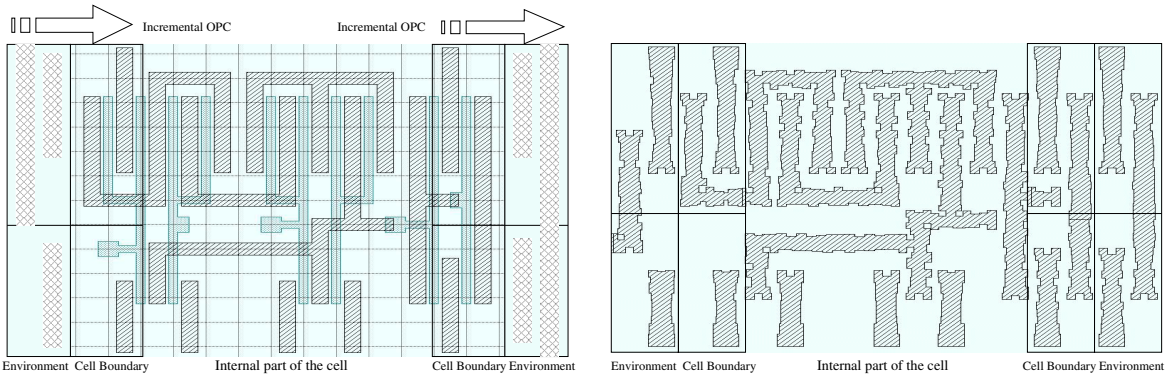
To create the library storing the corrected cell layouts, each cell is corrected in the presence of representative environments that model the optical influence of all potential neighboring cells. A representative environment consists of two columns that model the boundary region of the neighboring top or bottom sub-cell. The second column (the column further from the cell edge) has either a metal track running the length of the column or it is left empty. The first column feature is chosen from the set of six features, four depending on whether it is the top or bottom sub-cell and two that span both sub-cells. The first column features are limited due to the standard cell library characteristics, as shown in Figure 4. There are 12 possible feature combinations representing unique neighboring cell environments for the top or bottom sub-cell on both the left and right side. Therefore, every cell is corrected a total of 48 times to determine the boundary region OPC, using all 12 combinations on all four boundary regions.

In addition to the target geometries and representative environments, vertically oriented 20nm scattering bars with an equivalent fixed pitch to metal 1 were added to the correction environment. Fixed pitch scattering bars were used to enforce further regularity, ensuring equivalent distance between features and scattering bars regardless of placement. In this strategy every vertical pitch location is occupied by either a feature or a scattering bar. After the correction is completed the boundary area correction geometries of the corresponding sub-cells are stored.

To ensure consistent correction, adjustments were made to a commercial OPC algorithm. These adjustments were necessitated by the intended simplification which isolates a representative environment from the cell it represents. This complication arises because edge adjustments to correct feature printing will themselves have a non-negligible effect on neighboring features. If a feature is OPC corrected, a nearby feature corrected afterwards will be affected by the adjustment of the first feature. This is not a problem using full-chip correction, because all geometries and their environments are considered together during correction. However, when the OPC correction is done before layout and the results are later patched together, incongruities in the corrected environments occur.

In the presented method this is a problem because the inner geometries of the boundary cells are assumed to be interchangeable. The features in the neighboring cells outside of the boundary region are not present during correction. Due to the lack of optical influence these features would provide, there is a general shift in the corrected features toward the missing neighbor cell features. When correcting for the boundary columns on the left side of the cell the features expand to the left. Similarly, when the right boundary columns are corrected the features expand further to the right towards the missing right cell. When these two cells, corrected independently, are brought together in a real layout, the cell on the left is weighted too heavily towards the right and the right cell is weighted to the left. This causes an imbalance in the center creating over exposure on the abutting geometries.

To alleviate this problem an incremental approach is developed. For both the right and left boundaries, an equivalent starting point is selected and a column by column correction is performed incrementally moving rightward. This column by column approach enforces a general shift to the right in the correction geometries. This shift is due to a feature expanding slightly rightward compared to normal conditions because the feature on its right has not yet been corrected and is more narrow then it will be after correction. The first column to be OPC corrected for the boundary on the left side of the cell is the outer column of the representative environment. For right boundary correction, the second column from the right edge within the cell is the starting column. These starting positions were chosen because if cells are directly abutted the representative features model the first and second columns from the cell edge. Choosing the outer representative environment column for the left boundary is therefore equivalent to choosing the second column from within the cell for the right boundary. Another way to view this approach is that any time two cells are directly abutted, four columns interact in an appreciable way, two from each cell. For consistent OPC the first column corrected is the leftmost of these four interacting columns and the correction moves incrementally rightward. During left boundary correc-



(a) Incremental OPC on boundaries of NOR4X1 (b) An OPC-ready NOR4X1 in placement

Fig. 5. (a) Incremental OPC is performed on cell boundaries according to different environment. (b) Four cell boundaries are selected and stitched to the internal part of cell based on neighboring features during placement.

tion the left most of the four columns is the outer representative column. For right boundary correction the left most of these columns is the second column from the cell edge within the cell. The rightward progression, in both left and right boundary cases, also includes revisiting previously corrected features to account for the subsequent correction of nearby features.

Special consideration must be taken if a cell has a width of three or fewer columns. The boundary regions are two columns wide, therefore if a cell has a width of three or less the left and right regions overlap. A truncation approach is proposed to resolve these cases, which only the outer most column is substituted based on neighboring boundaries. Cells with widths of three also require substituting the middle column. This is done similar to the normal method in which internal structures are corrected independently of neighboring cells.

The boundary-based cell design methodology is shown in Figure 5. This cellwise OPC methodology can be embedded into current design flow. With top and bottom sub-cell breakdown and limited boundary features, each cell has 48 boundaries and one internal part after cellwise OPC. Once the placement is done, the internal parts of cells are directly from the OPC-ready library. The boundaries are picked according to their neighbor cell types. No further OPC is needed. Since the number of boundaries for each cell is fixed, the total number of cells in OPC-ready library is proportional to the number of cells in original library.

IV. Experimental Results

A representative library of ten cells was laid out applying the boundary-based cellwise OPC method stated in Section 3. A commercial RET software tool is used to perform the model-based OPC in the library design. A threshold based aerial image intensity model was used to determine simulated edges. The lithography system was dry (not immersion based) with a wavelength of 193nm and 0.95 NA. The illumination source was of quasar type with an illumination angle of 30 degrees, sigma out of 0.85 and sigma in of 0.55. A scalar diffraction model was chosen over a vector one, due to its proven accuracy in aerial image intensity models. A 4x reduction factor was chosen based on the ITRS roadmap [6].

A functional layout tool was developed to simulate representative full-chip standard cell designs. The simulated layouts consist of randomly selected cells abutted along rows. Rows are alternatively flipped to enable the sharing of power and ground. The cells are placed on a grid determined by the set pitch. All EPEs are reported on the metal 1 layer; for the results below we chose an experimental width of 80nm. The layouts are simulated using an aerial image intensity model. Each test performs EPE measurements of all features on 100 separate layouts. Measurements are taken at the center point of each grid box in the boundary regions that contain mask geometries. Only boundary geometries were considered because they are the areas in which the boundary based method offers potential improvement over a cellwise approach that does not consider neighboring cells. This will in turn increase the average EPE because more printing error will occur in the boundary regions. Power and ground lines are not included in these simulations due to the additional optical simulation they require while producing negligible net effect on the overall result. It is implied, however, that these lines can be included on metal 1 if desired.

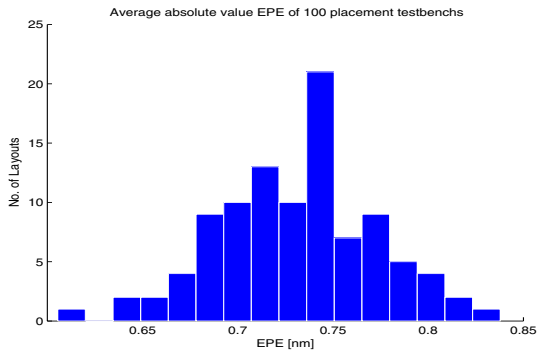
To offer a comparison and to motivate the need for an environment specific approach, non-patterned based simulations were also run. The cells were OPC corrected in an isolated environment, with scattering bars inserted at the standard size and spacing. Entire cell corrections were instantiated on cells in a similar layout method as described above but with no regard given to neighboring cell type. These layouts were simulated with the same aerial image intensity model as the boundary based approach. The most significant difference is found comparing the maximum positive EPE, average positive EPE, and maximum width. The increased width of the simulated features results from the additional optical influence of the neighboring cells. The cells were OPC corrected in isolated environments, but in full chip layout they have neighbors, resulting in constructive optical influence that has not been compensated for during correction.

It is evident from our comparison that the cellwise OPC without boundaries is unacceptable. The overall average positive EPE for non-boundary based simulations was 4.67nm,

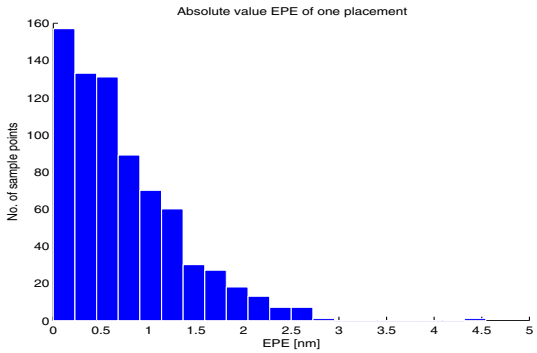
Test Case	No. of Gates	GDSII File Size (KB)			runtime (s)		
		Full-chip	Cellwise	Reduction	Full-chip	Cellwise	Reduction
1	625	2963	482	6.1X	7270	104	70X
2	1000	4848	501	9.7X	20800	202	103X
3	5000	23108	652	35X	21162	776	27X

TABLE I

SPEED-UP AND DATA VOLUME REDUCTION FROM PROPOSED METHOD. THE DATA SIZE OF CELL LIBRARY (10 CELLS) IS 451KB. TEST CASE 1 AND 2 WERE PERFORMED ON A SINGLE CORE PENTIUM XEON 2.4GHZ. CASE 3 WAS TESTED ON DUAL CORE PENTIUM XEON 3GHZ. FULL-CHIP OPC WAS PERFORMED BY CALIBRE [5]. CELLWISE OPC USED THE TCL SCRIPT IN CALIBRE WITHOUT PARALLEL OPTIMIZATION.



(a) Average absolute value EPE of 100 placement tests.



(b) Absolute EPE distribution in one placement

Fig. 6. (a) is the average absolute value EPE of 100 placement tests. (b) shows the EPE in boundary columns, most EPE are less than 2nm. The average EPE is 0.71nm and maximum EPE is 4.54nm.

while the maximum possible width ranged to 109.1nm, an error of more than 37%. These errors will increase with future technology nodes as the relative range of interaction increases, making it compulsory to develop an environment specific approach.

Using boundary-based cellwise OPC, Results are very promising: the average EPE for all metal1 features in 100 layouts is 0.731nm which is less than 1% of metal1 width as shown in Figure 6. We also analyze the maximum error on a per layout basis, sampling the maximum and minimum width on each layout. The average over all 100 layouts for the maximum width is 88.3nm and the average for the minimum width is 71.6nm. The maximum positive EPE was 7.2nm while the maximum width was 89.6nm. These maxima indicate that we did not just give the appearance of accuracy by smoothing over inconvenient data points with an average. Our proposed method has a 6X improvement on average EPE and 2X improvement on maximum width error over non-boundary based approach.

We also show the improvement on runtime and data size over full-chip OPC methodology in Table IV. As another extension of the cellwise OPC in [1], our boundary-based approach has a clear improvement on the method in [2], which has 5.5X speed-up and 2.5X data volume reduction.

In summation the results enforce the feasibility of a boundary based approach to cellwise correction. The correction produces substantially more accurate correction then obtained using an approach that is not dependent on neighboring cells.

V. CONCLUSION

The boundary-based approach is a promising method allowing cellwise OPC correction of standard cell layouts on future technology nodes. Cellwise correction was performed in the presence of representative environments, allowing corrected boundary features to be conditionally substituted based on the neighboring cells in full-chip layout. This method resulted in comparable accuracy to the full-chip approach, while producing many additional benefits, including reduced processing time, smaller layout memory requirements, improved correction accuracy, and the prevention of unrealizable fabrication conditions.

REFERENCES

[1] P. Gupta, F.-L. Heng, and M. Lavin, "Merits of cellwise model-based OPC," in *Design and Process Integration for Microelectronic Manufaturing II, Proc. SPIE 5379*, pp. 182–189, 2004.

[2] X. Wang, M. Pilloff, H. Tang, and C. Wu, "Exploiting hierarchical structure to enhance cell-based RET with localized OPC reconfiguration," in *Design and Process Integration for Microelectronic Manufaturing III, Proc. SPIE 5756*, pp. 361–367, 2005.

[3] L. Capodieci, P. Gupta, A. B. Kahng, D. Sylvester, and J. Yang, "Toward a methodology for manufacturability-driven design rule exploration," in *Proc. of the 41st conference on Design automation*, pp. 311–316, 2004.

[4] A. K. K. Wong, *Resolution Enhancement Techniques in Optical Lithography*. SPIE Press, 2001.

[5] Mentor Graphics, *Calibre Model-Based OPC Users Manual*.

[6] ITRS, "International technology roadmap for semiconductors 2004," tech. rep., 2004.