Fast Decoupling Capacitor Budgeting for Power/Ground Network Using Random Walk Approach*

Le Kang, Yici Cai, Yi Zou, Jin Shi, Xianlong Hong
Department of Computer Science and Technology,
Tsinghua University, Beijing, P.R.China

Sheldon X.-D. Tan
Department of Electrical Engineering, University of California at Riverside, USA

Abstract - This paper proposes a fast and practical decoupling capacitor (decap) budgeting algorithm to optimize the power ground (P/G) network design. The new method adopts a modified random walk process to partition the circuit. Then, by utilizing the isolation property of decaps, this new method avoids solving the large nonlinear programming problem in traditional decap optimization process. Also, this method integrates leakage currents optimization algorithm using a refined leakage model. Experimental results demonstrate that our proposed method achieves approximate a 10X speed up over the heuristic method based on sensitivity and only about 6% decap area deviation from the optimal budget using the programming method.

I Introduction

According to the roadmap of ITRS-2005 [1], robust P/G delivery network is considered as one of the grand challenges as technology scales down to 90nm and below. The improper design of power distribution system can degrade the circuit reliability and cause functional failures due to excessive IR drops, *Ldi/dt* noise, electro-migration and resonance effects. Power problems that are caused by rising frequency and continuing pushing for more device integrations will lead to exponential growth of the design and verification complexity of P/G networks.

Driven by the importance of the robust P/G delivery network, many methods have been proposed to guide the design of the P/G networks. Excessive IR drops and the increasing dynamic voltage fluctuations can be captured by many circuit simulation methods, such as hierarchical and macro-modeling based method [2], subspace projection based approach [3], random walk based approach [5] and etc. In order to remove excessive IR drops, wire sizing is typically employed in [7], however dynamic voltage fluctuations may still occur even if the wire sizing strategy is performed. In this case, adding decoupling capacitors is a suitable way to reduce dynamic noise. According to the modeling of P/G network shown in Fig.1, decap provides reservoir capacitor between power and ground.

However, decap budgeting of the P/G network is a difficult task because of the unbearable run time of the whole chip transient simulation. In [8] [9], the authors use nonlinear optimization program and conjugate gradient algorithm to acquire the optimal decap allocation under given constraints. In each step of conjugate gradient algorithm, numerical analysis should be applied to compute the sensitivity of the P/G network, which makes the time efficiency of the nonlinear optimization to be a big problem. As the experiment results shown in [9], the optimization process of a one million node circuit lasts more than 8 hours on a high performance workstation. Partitioning-based conjugate gradient method [10] has been proposed to optimize several small circuits instead of the whole circuit. But the partitioning-based method also has to solve the nonlinear programming problem by carrying out the linear system simulation in each step. On the other hand, the possible deviation from optimal result of budgeting may be significant. It is still far away from practical use for industry application due to its complexity. If leakage effect is considered, over-adding decaps may increase power consumption significantly. Therefore, in [11], leakage effects of the decap was considered, but the leakage model it use was a little bit over-simplified for practical use.

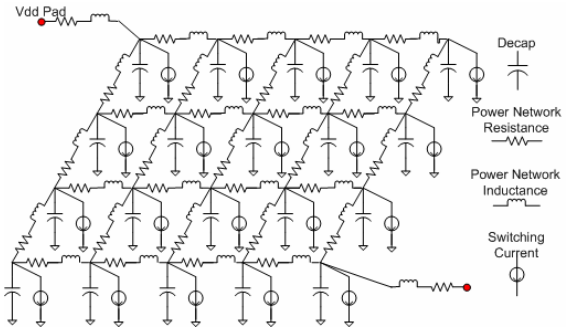

Fig. 1. Model of Power/Ground Network

In this paper, we propose a fast and practical decap budgeting algorithm to optimize the dynamic performance of P/G network. The new method uses a modified random walk process to partition the circuit, and utilizes the isolation property of the decaps. First, decaps are planted at the boundary of each sub-circuit, which can isolate each sub area very well. Then instead of solving the global programming problem, we use preconditioned conjugate gradient approach (PCG) method to get the near optimal solution in each sub area. Because the random walk method gives out very good boundaries to plant the decaps, global dynamic performance highly relies on the performance of each individual sub area. On the other hand, the PCG method is efficient in finding out the optimal solution

*This work is supported by NSFC No. 90307017.

1-4244-0630-7/07/$20.00 ©2007 IEEE.

especially when problem size is small. Thus, the quality of local solution is improved. Finally, considering the overhead of decap planting at the boundary and the improvement of decap usages in local area together, we find that the design quality can be improved a lot within a few run time.

Our contributions are: (1) Special random walk method is used to find out an optimal partition boundary to plant decaps. (2) We find out that trying to improve the local solution quality and sacrifice the design quality at the boundary will improve the time efficiency a lot than trying to improve the global solution quality. (3) A more accurate leakage model of decaps is integrated in our optimization flow to make the method more practical for application.

This paper is organized as follows: Section II gives a basic review of random walk principle. Section III presents how to use random walk principle in our proposed optimization method according to the localization property. Section IV gives out the refined model of the decap leakage current. Finally, Section V concludes the paper.

II. Review of Random Walk Process

In [5], random walk process was introduced to P/G network analysis. Distinguished from the traditional simulation methods via solving the matrix equation, random walk principle is a statistical winning process. The circuit illustrated in Fig.2 can be written as the following formula (1) according to Kirchoff current law and nodal equation.

$$V_x \sum g_i - \sum g_i V_i = -I_s \quad (1)$$

Then we will have,

$$V_x = \sum \frac{g_i}{\sum g_i} V_i - \frac{I_s}{\sum g_i} \quad (2)$$

If we define the coefficient $g_i / \sum g_i$ to be $p_{x,i}$, then we can get $\sum p_{x,i} = 1$. Thus, $p_{x,i}$ can be treated as the probability of walking from node *x* to node *i*. This means that the constant $-I_s / \sum g_i$ can be treated as the cost we should pay at node *x*. When achieving the home nodes (pad nodes in P/G network) at the end of winning process, we can calculate the total cost by summing the cost paid at each step. It has been proved that the average cost from one node to the home node in random walk process is equal to the node voltage calculated by traditional P/G network analysis process [4]. Thus, we can play the walking-game for a certain number of rounds, then calculate the average cost to calculate node voltage in a statistical way.

We have implemented the random walk algorithm [6]. As shown in Table I, for a specific node of the test circuits, we compare the accuracy and run time from random walk algorithm (RW) with that of standard PCG method. Here the

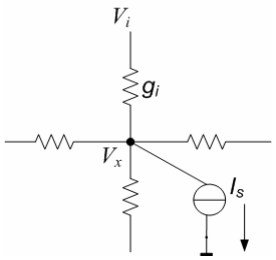

Fig. 2. A representative part of P/G networks.

PCG results are considered as the correct solution to do the comparison. The results for different test cases show that the performance in terms of CPU time of RW is much higher than PCG approach. Also, for RW, the max absolute error margin is just about 11 mv, and the max relative error is approximately 0.6%. That is to say, using random walk approach can gain one order of magnitude speedup over PCG. method.

More importantly, comparing with the flat PCG, which is used for solving the whole network, the random walk process only obtains the specific node voltage. The obvious advantage is that it gets solutions for a portion of the large P/G networks without solving the whole circuit, but the speedup only suits for a single node or a small number. If we use random walk to calculate the whole circuit with few Vdd pads, the performance may be poor. And it is also difficult to use it to solve the transient analysis problem, because the linear model of dynamic elements deduced by Norton Companion model should be updated in each simulation step. In other words, if we use random walk approach to solve all the nodes in transient analysis, it may not be very effective on analyzing the voltage variation for decoupling capacitor budgeting.

III. Random Walk based Approach for Decap Allocation

In this section, we mainly explain the idea of isolation decap planting strategy, the employ of random walk process to partition the whole network, and the iterative method to budget decaps in P/G network.

TABLE I Comparison with PCG in Terms of Speed and Accuracy.

Circuit Size	Run Time		Accuracy			
	PCG (s)	*Random Walk (s)*	*PCG (v)*	*Random walk (v)*	*Absolute Error(mv)*	*Relative Error*
100	0.001	<0.001	1.998032	1.998423	0.391	0.02%
1600	0.021	0.002	1.944538	1.940454	4.084	0.21%
6400	0.146	0.015	1.901242	1.907516	6.274	0.33%
25600	1.224	0.108	1.853241	1.861951	8.710	0.47%
102400	10.816	1.140	1.740406	1.751299	10.893	0.63%

A. Isolation Decap Planting

Usually, the frequency of noises in P/G network is high. Therefore, enough decaps will provide good fast return paths for noise current, this is why adding enough decaps can reduce noise level. On the other hand, under a special noise frequency, we can calculate how many decaps is enough to provide good isolation in P/G network even in time domain.

Our decap planting technique is based on the following observation. Due to high via density in M1, the noise current inside local area usually not propagate along with the rail but trends to go up to M2 first from the vias. Then if no decaps is planted to provide fast current return path, it will go to up layers until the pad is reached. This usually causes long current paths and makes the dynamic drop obvious. However, the higher metal layer the noise current goes, the smaller voltage drop it can causes due to small metal resistance. So, if we can reduce the path length in M1 and M2, it is enough to reduce the noise level obviously.

Definitely, the worst case is the current sources inside the local area turn on simultaneously. In this case, we should find out some boundary nodes that do not consume large dynamic current during this time period and plant enough decaps to provide fast current return path. Later we will introduce our method to find out such kinds of boundary. Here we just suppose all the boundary nodes are given.

Then we can calculate the average current per each node inside the local area according to the piece wise liner (PWL) model of all the current sources. Suppose the internal node i contains a switching current whose average current is $\overline{I}_i$, we will plant a decap at the boundary node with its capacity C_i satisfying equation (3).

$$\overline{I}_i - \frac{2C_i}{h} \times V_i^{(dc)} = 0 \tag{3}$$

In equation (3) above, $\overline{I}_i$ is the average current of internal node I during a time period h, and $V_i^{(dc)}$ is the voltage of node i in DC analysis.

If the boundary condition is good enough, the planted decaps will isolate every sub-area perfectly and each of them can be taken into consideration independently.

Here we use a transient simulation tool to compare the IR drops of each node inside the sub area before and after planting process. The results are shown in Table II.

In Table II, columns 1, 2, 3, 4 represent the sub area ID, the internal node number of each sub area, the total node number of the P/G network, and the maximum voltage drop before planting boundary decaps respectively. The last two columns represent the maximum voltage drop after planting, and the number of nodes in the sub-circuit whose IR drops have been improved. From these results, we can observe that, after planting decaps, the maximum dynamic IR drop in the sub-circuit has been reduced obviously and nearly all the nodes' voltage drops have been improved. In other words, even if we only plant decaps at the boundary, the dynamic performance of each sub area can be improved.

.

TABLE II The Voltage Drop Comparison before/after Using the Boundary Allocation Strategy

Sub area	Node Num	Total Node Number	Max Vol Drop(mv)	Optimized Boundary	
				Max Vol Drop(mv)	Improved Node Num
1	11	744	203.62	30.83	10
5	46	7492	260.47	72.06	46
14	124	32112	315.71	135.19	122

B. Partition Based on Random Walk Process

As we mentioned in above section, the planting decaps at the boundary node can improve the dynamic performance of internal nodes. However, if unluckily the violation node (whose voltage is below the threshold) locates at the boundary, it will be hard to optimize because the planted decaps will not get enough charge. So in this part, we use a modified random walk process to partition the circuit which makes the violation nodes locate inside the sub-circuits.

Firstly, we adopt the conjugate gradient (CG) solver based on incomplete cholesky decomposition as the transient analysis simulation tool. So the nodes with excessive dynamic drop violation are gained.

Then the modified random walk process is applied from each violation node. In our new method, the violation node is considered as the beginning node, and the probability in the walking process is also treated according to Section II. But differently, the cost of every node mentioned in the random walk analysis is ignored. In the modified walking process, our brief target is to achieve the boundary of walking process. After performing the walk process several times, the nodes accessed from beginning node have been recorded so that the boundary for each violation node can be gained by the recorded nodes. Fig. 3 gives out the example of the boundary by our proposed method. We observe that

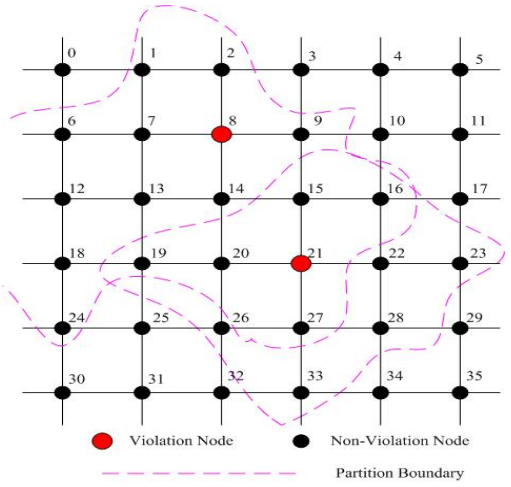

Fig. 3. The Boundary Gained by the Modified Random Walk Process

node 8 and 21 are violation nodes and the boundaries are given by dashed lines. From node 21, we may achieve the partition containing 11 nodes through the walking process.

After we finish the walking process from each violation node, the boundary of each violation node is gained. But in the circuit, the violation nodes always lay close to each other. As shown in Fig. 3, the partitions, acquired by node 8 and 21, are not separated. So it is essential to merge the partitions that intersect each other and calculate a new boundary.

At last, intersected sub-circuits are merged together. For each sub-circuit generated from the partitioning, we use localization property to solve decaps budgeting separately.

C. Decap Budgeting Flow Based on Random Walk Process.

The whole decaps budgeting flow based on modified random walk process is shown in Fig. 4.

```
Decaps flow based on Random Walk Process
1. Solve the circuit, and identify the violation nodes;
2. While (violations) {
3.    For each violation node {
4.       Apply modified random walk process;
5.       Form the partition in the walking process}
6.    Merge the partitions that intersect each other;
7.    Use boundary allocation strategy for each partition;
8.    Update all the decaps and solve the new circuits}
9. Optimization Successful.
```

Fig. 4. Decaps flow based on random walk process.

In the optimization flow, we only apply transient simulation at two places. One is at the very beginning to solve the circuit, and get all the violation nodes. The other is at the end of every optimization step to check the updated circuits and verify the optimization result. Comparing with the decaps budgeting methods which need to carry out long time to construct the adjoint network, compute the sensitivity of object function and solve the nonlinear programming, the method proposed in this paper make use of random walk process, but avoids complex computation for adjoint network etc. And also the decap budgeting problem using random walk process has smaller iterative times that demonstrated by experimental results.

By using this decaps budget flow, we did experiment on a 744 node circuit named u_cnt100. Results in Fig. 6 are very similar to Fig. 5 using a heuristic method based on sensitivity which is also mentioned in [9]. Further discussions on our proposed method are given in Session V.

IV. Refined Leakage Current Model for Decaps

Usually, decaps in different levels (on-board, on-package and on-die) are used together to reduce dynamic voltage noise of different frequencies [12]. Since large on-chip poly-insulator-poly or metal-insulator-metal decaps tend to consume large die area, in power/ground designs, on-chip decaps are usually made of MOS transistors with source and drain connected together [11]. Since the oxide thickness T_{ox} is smaller than 20Å in nanometer design, the gate leakage of MOS-based decaps will become more significant. As a result,

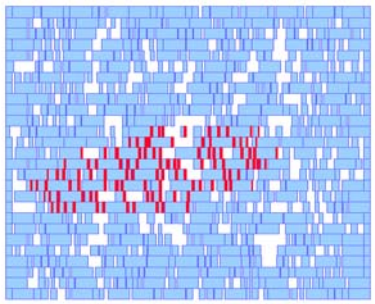

Fig. 5. Decap Allocation Result of the Heuristic Method

adding decaps will hurt power consumption, which in turn will make the added decaps less effective to reduce the voltage drops. The leakage current of the MOS-based decap can be formulated as [11] [13]:

$$I_{gate} = k \times (\frac{V}{Tox})^2 \times e^{-\alpha \cdot Tox/V} \times w \qquad (4)$$

where α and k are parameters related to specific technology , w is the gate width of NMOS (or PMOS) while T_{ox} is oxide thickness and V is the supply voltage.

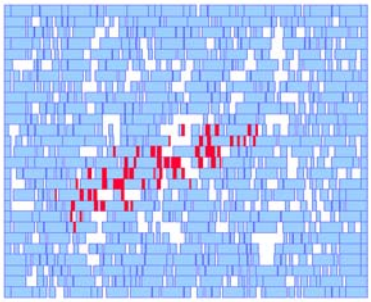

Fig. 6. Decap Allocation Result of the Proposed Method

It is shown in the formula that the value of I_{gate} is the

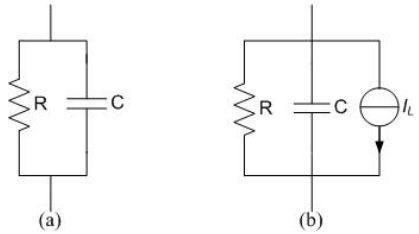

Fig. 7. Two Equivalent Models for Decaps Leakage

exponential function of the supply voltage V. To consider the leakage current of decaps, as shown in Fig. 7(a), the leakage model used in [11] is a little bit over-simplified which only contains a constant resistor besides the decap, but the exponential effect is not considered.

In this section, we use an approximate leaky decap model to analyze gate leakage current for MOS-based decaps. As shown in Fig. 7(b), we propose a more accurate leakage decap model containing a resistor, a capacitor and a time-variant current source, which uses the piece wise liner model, to capture the main leakage current.

TABLE IV
Experimental Results Compared to Existing Heuristic Budget and Optimal Budget Method.

Circuit Name	#Node	#violation	Heuristic Budget		Optimal Budget		Random Walk Based		Speedup On Heuristic	Deviation from Optimal
			Time (s)	Aera of Decap(um^2)	Time (s)	Aera of Decap(um^2)	Time (s)	Aera of Decap(um^2)		
u_cnt100	744	96	37.34	7182.58	117.08	6779.66	7.81	7190.24	4.8	6.06%
u_cnt500	3741	665	223.59	44938.03	961.42	42372.17	33.14	45072.39	6.7	6.37%
U05614	32112	3682	2812.04	176975.84	8709.37	169491.63	370.96	178290.51	7.6	5.19%
U19649	112392	10755	11834.1	728931.47	39257.62	677966.08	958.63	721091.26	12.3	6.36%
U28070	1618026	612132	28596.4	8922309.20	NA	NA	1606.54	9142708.72	17.8	NA

TABLE III Violation Node Statistics Comparison to the Simplified Model when our New Model is Considered. VN = Violation Node

Circuit Name	Node Num	Eliminated VN Num	VN Num	Newly VN Num Using Our Model
U_cnt100	744	102	0	2
U_cnt500	3741	679	0	9
u05614	32112	3977	0	26

After the circuits are optimized with the simplified leakage model, we introduce our leaky model to P/G grid and apply transient simulation to verify whether the violation nodes still exist. The analysis results are shown in Table III. From the results, we can observe that, although the optimization process with the simplified leakage model, reduces the violation node (VN) number to zero, new violation nodes still appear when our new leakage model is considered since the over-simplified model did not consider the exponential relation between the leakage current and the supply voltage. In order to maintain a robust optimization for P/G network, the decap leakage current model must be sufficiently accurate.

We still use the two-stage P/G optimization method [11] to do with our modeling. First, it optimizes the dynamic voltage noise assuming all decaps are leakage free, and then in the second stage, in order to compensate the IR drops caused by leakage currents, it performs a wire sizing strategy using a branch and bound method to minimize the added wire area.

V. Experiment

We implement our presented algorithm in C++ programming languages. All the experimental results are obtained on a *SUN UltraSparc* workstation V880 with 1GHz CPU and 4GB memory. All test cases are real industry standard-cell circuits with pre-placement information in LEF/DEF format. Those circuits have complexities ranging from 744 nodes to 1.6 million nodes.

To demonstrate the efficiency of our proposed optimization algorithm in Section III, we compare it with the existing sensitivity-based heuristic method and optimal budget method using nonlinear programming [9]. To make comparison possible, we test on the same circuits with same parameters and constraints. Table IV summarizes the comparison, where columns 1, 2, 3 represent circuit name, total node number, and violation node number respectively. And the last two columns, compares the random walk based method with the heuristic method in terms of CPU times and the optimal budgeting in the decap area. From Table IV, we can find that our proposed method is usually 10 times faster than the heuristic method which is considered as an extremely fast approach, and it only has about 6% decap area deviation with the optimal budgeting.

Then we introduce both the simplified leakage model and our proposed model to the test cases after they are optimized by the random walk based flow. In the second stage, we try to detect the most sensitive nodes to perform the wire sizing strategy. In [11] it has been proved that the wire sizing strategy is not very time consuming. So the extra run time in the second stage may be ignored. We compare the optimization results between the simplified leakage model and our newly proposed accurate model. The comparison about the routing resource increase is shown in Table V. From the result, we can see that our proposed leakage model, which considers the exponential effect, occupies a little more routing resource than the simplified model, and the relative deviation is within 1%. But our proposed model makes the optimization process more practical for use.

VI. Conclusion

This paper propose an extremely fast decap optimization based on the idea of using random walk approach to find out the best partitions which utilize the localization property and then adding decaps on these boundary of partitions. The experimental results on the industry test cases demonstrate that the proposed method based on random walk process achieves approximate a 10X speed up over the heuristic approach, and a test circuit with 1.6 million nodes can be carried out within half an hour on the *Sun Workstation*. Then the paper considers a refined leakage current model for

decap. The combination of the proposed optimization process and two-stage method for accurate leakage current can efficiently optimize power/ground network in real industry design.

TABLE V
Optimization Result Comparison between Two Leakage Models using the Two-Stage Method

Circuit Name	#Node	Added Decap without Leakage (um^2)	Ratio of Routing Resources Increases	
			Simplified Model	Our Accurate Model
u_cnt100	744	7190.24	1.85%	1.88%
u_cnt500	3741	45072.39	5.83%	5.86%
u05614	32112	178290.51	3.00%	3.25%
u19649	112392	721091.26	4.91%	5.14%

References

[1] The International Technology Roadmap for Semiconductors (ITRS), http://public.itrs.net/, 2005 update.
[2] M.Zhao, R.V.Panda, S.S.Sapatnekar and D.Blaauw, “Hierarchical analysis of power distribution networks”, IEEE Trans. On Computer Aided Design, vol. 21, no. 2, pp. 159-168, Feb. 2002.
[3] Y. Cao, Y. Lee, T. Chen and C. Chen, “HiPRIME: Hierarchical and Passivity Reserved Interconnect Macro-modeling Engine for RLKC Power Delivery”, In Proceeding of IEEE/ACM Design Automation Conference, pp. 379-384, New Orleans, Jun. 2002.
[4] P.G. Doyle and J.L. Snell, “Random Walks and Electric Networks.” arXiv: math.PR/0001057
[5] H.F. Qian, S.R. Nassif, and S.S. Sapatnekar, “Random walks in a supply network,” in Proc. Design Automation Conf., 2003, pp. 93–98.
[6] Le Kang, Yici Cai, Jin Shi and Xianlong Hong, “In-depth Exprimental Study of Power Grid Network Analysis using Random Walks Algorithm”, International Conference on Communications, Circuits and Systems, 2006
[7] T. Mitsuhashi and E.S. Kuh, “Power and Ground Network Topology Optimization for Cell Based VLSIs”, Proc. 29th ACM/IEEE Design Automation Conference, pp. 524~529, 1992
[8] H. Su, S. S. Sapatnekar, S. R. Nassif. “An Algorithm for Optimal decoupling Capacitor Sizing and Placement for Standard Cell Layouts”. In Proc. International Symposium on Physical Design, pages 68-73, San Diego, CA, April 2002
[9] J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan, and Z. Pan, “A fast decoupling capacitor budgeting algorithm for robust on-chip power delivery,” in Proc. Asia South Pacific Design Automation Conf. (ASPDAC), Jan. 2004, pp. 505–510.
[10] H. Li, Z. Qi, S. X-D. Tan, L. Wu, “Partitioning-based approach to fast on-chip decap budgeting and minimization”, Proc. IEEE/ACM Design Automation Conference (DAC’2005), pp. 170-175, CA, 2005
[11] Jingjing Fu, Zuying Luo, Xianlong Hong, Yici Cai, Sheldon X.-D. Tan, Zhu Pan, "VLSI On-Chip Power/Ground Network Optimization Considering Decap Leakage Currents", 2005.1, The 10th IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC2005), Shanghai, China, p735-738
[12] D.J. Herrell, B. Beker. “Modeling of Power Distribution Systems for High-Performance Microprocessors”, IEEE Transactions On Advanced Packaging, August 1999, 22(3): 240-248
[13] Kim N.S., Austin T., Baauw D., Mudge T., Flautner K., Hu J.S., Irwin M.J., Kandemir M.; Narayanan V. “Leakage current: Moore's law meets static power”, IEEE Transaction on Computer, Volume 36, Issue 12, Dec. 2003: 68 – 75