ARM MPCore

The streamlined and scalable ARM11 processor core

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Abstract - The required processing performance of embedded processor core is getting higher and higher without increasing power consumption dramatically. In same time, large SoC design has more risk of re-spin and long design time due to the complexity and difficulty of verification. ARM offers multi core solution to overcome such a situation over various applications.

Introduction

ARM11™ MPCore™ synthesizable processor implements the ARM11 microarchitecture and can be configured to contain between one and four processors delivering up to an aggregate 2600 Dhrystone MIPS of performance.

Providing a scalable solution, the ARM11 MPCore processor provides existing software portability across single CPU and multi-CPU designs. The ARM11 MPCore processor provides enhanced memory throughput of 1.3Gbytes/sec from a single CPU, and a solution that delivers greater performance at lower frequencies than comparable single processor designs, offering significant cost savings to system designers, while maintaining full compatibility with existing EDA tools and flows. The ARM11 MPCore processor also simplifies otherwise complex multiprocessor design, reducing time-to-market and total design cost.

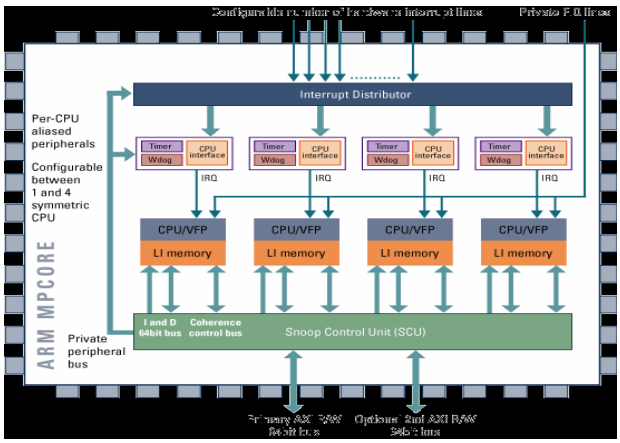

Fig 1. ARM11MPCore block diagram

The ARM11 MPCore processor supports a fully coherent data cache, providing the designer with a unique level of flexibility across various symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP), or any combination of either style of multiprocessor design. The MPCore processor increases a solution's performance via the ability to cache shared data, increases system responsiveness by allowing workloads to be balanced between processors with the portability of existing multitasked applications, and enabling scalability through efficient processor utilization for multithreaded applications, typical of the workloads of today's rich consumer devices.

The ARM11 MPCore processor provides the manufacturer flexibility to use the same core with different configurations for a range of products having various design requirements. The MPCore processor's consistent bus interfaces and scalable design also enables the performance and power advantages of a multiple processor design while also reducing the total costs and risks of delivering next generation digital devices.

The ARM11 MPCore processor supports the ARMv6 architecture, with SIMD media extensions for next-generation rich multimedia and convergent devices and ARM Jazelle® Java acceleration. It also features configurable level 1 caches, 64-bit AMBA AXI™ interfaces, Vector Floating Point coprocessors and programmable interrupt control and distribution. The processor supports Adaptive Shutdown of unused processors to give dynamic power consumption as low as 0.49 mW/MHz from a generic 130nm process excluding cache. ARM Intelligent Energy Manager (IEM) can further reduce consumption to as low as 0.30mW/MHz by dynamically predicting the required performance and lowering the required voltage and frequency. The ARM11 MPCore enables SoC designers to view the core as a single “uniprocessor”, simplifying SoC development and reducing time-to-market.

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Core area, frequency range and power consumption are dependent on process, libraries and optimizations. The example numbers showed in Table-1 are illustrative of synthesized cores using general purpose TSMC process technologies and ARM Artisan standard cell libraries and RAMs.

PERFORMANCE CHARACTERISTICS

	90 nm	
	Speed Opt	**Area Opt**
Configuration details	1 CPU	1 CPU
Standard Cells	Advantage-HS	Metro
Memories	Advantage	Metro
Frequency* (MHz)	620	320
Area with cache (mm²)	2.54	1.46
Area without cache (mm²)	1.80	0.90
Cache Size	16K/16K	16K/16K
Power with cache† (mW/MHz)	0.43	0.23
Power w/o cache† (mW/MHz)	0.37	0.18

* Worst case conditions - 0.9V, 125C, slow silicon
† Typical case conditions - 1V, 25C, typical silicon

Table-1 Example implementation

The speed optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve the target frequency performance. The area optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve a target area density. All figures include internal peripherals and interrupt system.

The cache sizes are specified as Instruction-Cache / Data-Cache. The area without cache numbers quoted exclude RAM area, but include all logic including memory management, cache control and debug. The area with cache numbers quoted includes the core, the specified instruction and data caches and all necessary RAMs.