Predicting the Performance and Reliability of Carbon Nanotube Bundles for On-Chip Interconnect

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Abstract— Single-walled carbon nanotube (SWCNT) bundles have the potential to provide an attractive solution for the resistivity and electromigration problems faced by traditional copper interconnect. In this paper, we evaluate the performance and reliability of nanotube bundles for future VLSI applications. We develop a scalable equivalent circuit model that captures the statistical distribution of metallic nanotubes while accurately incorporating recent experimental and theoretical results on inductance, contact resistance, and ohmic resistance. Leveraging the circuit model, we examine the performance and reliability of nanotube bundles including inductive effects. The results indicate that SWCNT interconnect bundles can provide significant improvement in delay over copper interconnect depending on the bundle geometry and process technology.

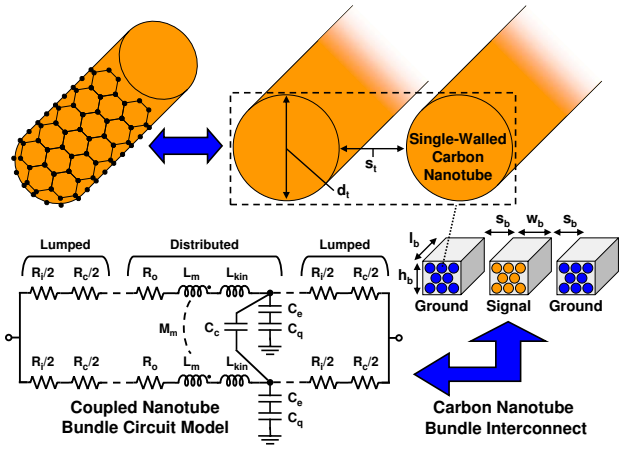

Fig. 1. System of SWCNT bundles implementing a signal line and two adjacent ground return paths, and the proposed RLC circuit model.

I. Introduction

The modeling, design, and implementation of on-chip interconnect continues to be a fundamental roadblock to realizing high-performance integrated circuits. As process technology scales and wire width decreases, traditional copper interconnect will suffer from increases in resistivity due to surface roughness and grain boundary scattering [1]. This will lead to both delay and electromigration problems [2]. Given the long-term scaling problems associated with traditional copper interconnect, radical alternatives are required. Single-walled carbon nanotubes (SWCNT) have been proposed as a possible replacement for copper interconnect due to their large conductivity and current carrying capabilities [3]. SWCNTs are rolled graphitic sheets that can either be metallic or semiconducting depending on their chirality [4]. Due to their covalently bonded structure, SWCNTs are extremely resistant to electromigration and other sources of physical breakdown [5].

While SWCNTs have desirable material properties, individual nanotubes suffer from an intrinsic ballistic resistance of 6.5 $k\Omega$ [6]. To alleviate the intrinsic resistance problem, bundles or ropes of SWCNTs in parallel, depicted in Figure 1, have been proposed and physically demonstrated as a possible interconnect medium [3, 7]. In the absence of special separation techniques [8], the metallic nanotubes are distributed with probability $P_m = 1/3$ since one-third of the possible SWCNT chiralities are metallic [4]. Given the desirable material properties of carbon nanotubes, the modeling and design of nanotube-based interconnect solutions for future VLSI applications is a crucial step toward the adoption of this promising technology.

In this paper, we provide a comprehensive analysis of the performance and reliability of SWCNT bundles for both local and global interconnect in future VLSI applications. We develop a scalable equivalent circuit model that captures the statistical distribution of metallic nanotubes while accurately incorporating recent experimental and theoretical results on inductance, contact resistance, and ohmic resistance [9–12]. We also describe a method for determining the optimal nanotube diameter for local interconnect applications. Leveraging the circuit model, we examine SWCNT bundle performance and reliability relative to copper technology including the impact of inductive effects for various bundle geometries and process parameters. The results indicate that SWCNT bundles can provide significant improvement in delay over copper interconnect depending on bundle geometry, individual nanotube diameter, and the statistical distribution of metallic nanotubes.

II. Previous Nanotube Interconnect Studies

Several previous studies have investigated nanotube-based interconnect. Burke introduced an RLC model for an indi-

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vidual SWCNT that models the nanotube as a 1-D quantum wire with a quantum capacitance, kinetic inductance, and a perfect contact resistance between the nanotube and its metal contacts [13]. Based on Burke's model, Raychowdhury and Roy developed a model for SWCNT bundles that included the additional resistance due to acoustic and optical phonon scattering [14]. Also leveraging Burke's model, Srivastava and Banerjee analyzed the impact of imperfect metal-nanotube contacts and discussed the increase in resistance when only a portion of the bundle's nanotubes are metallic [15]. Finally, Naeemi and Meindl proposed a mono-layer SWCNT structure for local interconnect and demonstrated that the high bias resistance due to optical phonon scattering will not have a large effect for most predicted interconnect geometries [16–18].

While these initial studies provide a good starting point for future research efforts, several important modeling considerations and their implications still need to be addressed. Previous studies have either assumed that all nanotubes are metallic [14, 16] or did not consider the performance and reliability implications of the statistical distribution of the metallic nanotubes in the bundle [15]. Furthermore, the new theoretical and experimental results presented in [9–12] demonstrate that the diameter dependence of the ohmic and contact resistances can have a drastic impact on performance, which has not been previously considered when evaluating SWCNT bundles.

Given the performance implications of inductive effects [19], accurately capturing the inductance of SWCNT bundle interconnect and its impact are crucial. For SWCNT inductance modeling, which consists of both magnetic and kinetic inductances, several previous studies did not model the magnetic inductance since it is predicted to be significantly less than the kinetic inductance for a single nanotube [14, 16]. However, the magnetic inductance can exceed the theoretical kinetic inductance in realistic interconnect geometries as we discuss in Section III-C. Furthermore, the kinetic inductance reported in experimental studies has been substantially lower than its theoretical value [20]. Other studies did not model the mutual magnetic inductance between nanotubes [15], which can lead to non-physical results [21]. Comprehensive inductance modeling techniques are needed to provide a holistic evaluation of SWCNT bundles for future VLSI applications.

III. Circuit Model for SWCNT Bundles

To evaluate SWCNT bundles for future interconnect applications, we have created an accurate and scalable RLC equivalent circuit model, which is displayed in Figure 1. Each SWCNT has lumped resistances representing both the intrinsic ballistic resistance (R_i) and an additional contact resistance (R_c) between the SWCNTs and on-chip metal components. A distributed resistance (R_o) captures the ohmic resistance of the SWCNT. C_e and C_c represent the electrostatic capacitance to ground and between SWCNTs, respectively. C_q is the quantum capacitance of the SWCNT. L_{kin} models the kinetic inductance. L_m and M_m represent the partial self and mutual inductances of coupled SWCNTs. In the following sections, we discuss the modeling of resistance (Section III-A), magnetic inductance (Section III-B), kinetic inductance (Section III-C), and capacitance (Section III-D) for SWCNT bundles.

A. Resistance

To model the ohmic and contact resistances for SWCNT bundle interconnect, we utilize the diameter-dependent model that we developed in [10]. For nanotubes operating in the low bias regime ($V_b \leq \approx 0.1V$), the total resistance is

$$R_{low} = R_i + R_c \; if \; l_b \leq \lambda_{ap} \quad (1)$$

$$R_{low} = R_o + R_i + R_c \; if \; l_b > \lambda_{ap} \quad (2)$$

where l_b is the bundle length [6], and λ_{ap} is the mean free path of acoustic-phonon scattering. For high applied bias voltages, the resistance is $R_{high} = R_{low} + V_b/I_o$, where I_o is saturation current of an individual nanotube. A recent worst-case analysis suggests that the bias voltage does not greatly impact the resistance unless the number of nanotubes in the bundle (n_b) is greater than 50 and $l_b < 10\lambda_{ap}$ [18].

The intrinsic resistance (R_i) of a ballistic SWCNT is $R_i = h/4e^2 \approx 6.5\ k\Omega$ [6]. Recent experimental and theoretical results have revealed that the contact resistance greatly increases when the SWCNT diameter (d_t) is less than 2 nm [10, 12]. We utilize the model in [10] to model the diameter dependence of the increased lumped resistance due to imperfect metal contacts. The ohmic resistance of an SWCNT is $R_o = (h/4e^2)(l_b/\lambda_{ap})$ [6]. Recent experimental evidence and theoretical formulations have demonstrated that λ_{ap} is proportional to d_t [10, 11]. The resistance of an individual SWCNT versus diameter is governed by $R_o = (h\alpha l_b T)/(4e^2 v_F d_t)$ where v_F is the Fermi velocity in graphene, T is the temperature in Kelvin, and α is the scattering rate [11]. Based on experimental measurements for λ_{ap}, the diameter-dependent equivalent ohmic resistivity of a SWCNT is

$$\rho_t = \frac{h}{4e^2 C_\lambda d_t} \quad (3)$$

where C_λ is the mean free path-to-nanotube diameter proportionality constant defined in [10]. The resistance of the SWCNT bundle, assuming no current redistribution due to magnetic inductance, is defined by the parallel combination of the individual SWCNT resistances, $R_b = R_t/n_b$, where R_t is the total resistance of an individual SWCNT. Note that we neglect the resistive interaction between nanotubes since the nanotube-nanotube coupling resistance has been physically measured to be significantly larger than R_i [22].

Neglecting the diameter-dependent nature of the ohmic and contact resistances can produce errors as high as 120% and 85%, respectively [10]. To examine the impact of the SWCNT bundle resistance for realistic interconnect geometries, we calculated the total resistance of dense SWCNT bundles for various l_b and bundle width (w_b) values when $d_t = 1.0\ nm$ [10]. For long bundles with $w_b = 22\ nm$, the SWCNT bundle resistance is 82% less than it is in scaled copper interconnect. The d_t value greatly impacts the relative improvement over traditional copper interconnect. For example, dense bundles with $d_t = 2.0\ nm$ have only a 22% improvement in resistance. SWCNT bundles are at a disadvantage for short l_b and large w_b values, when the contact resistance is significant [10].

For local interconnect, the l_b value for which the resistance of the SWCNT bundle equals that of copper interconnect for a

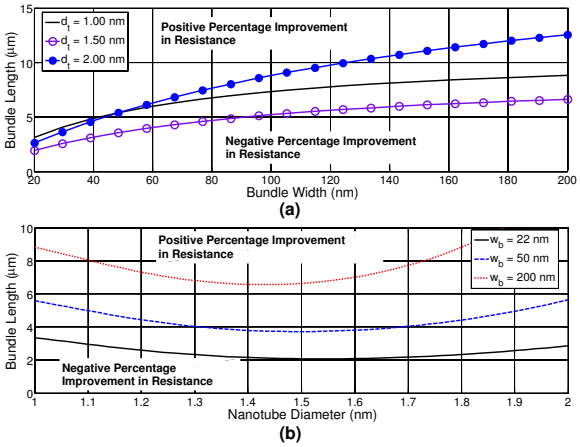

Fig. 2. Geometry where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various (a) l_b values and (b) d_t values.

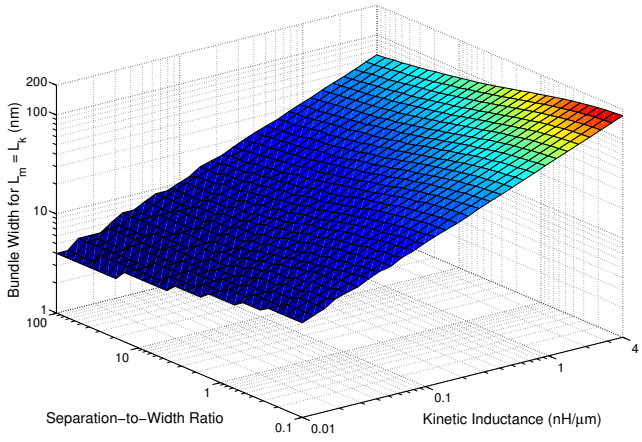

Fig. 3. Dense carbon nanotube bundle w_b values for which the theoretical magnetic and kinetic inductances are equal.

given w_b can be calculated by equating the resistance of copper and SWCNT bundle interconnect:

$$R_{Cu} - R_b = 0 \Rightarrow \frac{\rho_{Cu} l_b}{w_b h_b} - \frac{R_c + \rho_t l_b}{n_b} = 0 \qquad (4)$$

where R_{Cu} is the resistance of a copper conductor with the same dimensions as the bundle and ρ_{Cu} is the copper conductor's width-dependent resistivity. Solving (4) for l_b yields

$$l_b = \frac{R_c w_b h_b}{\rho_{Cu} n_b - \rho_t w_b h_b}. \qquad (5)$$

Using (5), the minimum length for which SWCNT bundle interconnect has an advantage over copper technology for a particular conductor geometry can be determined.

Figure 2a depicts the l_b and w_b values where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero based on (5). As d_t is decreased, the impact of R_c substantially increases. However, n_b increases as d_t decreases, which leads to lower overall resistance. Due to the interaction between these two conflicting trends, an optimum d_t value exists for a given w_b. Figure 2b depicts the l_b and d_t values where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various w_b values. The optimal d_t value for SWCNT bundles with short l_b values can be determined by minimizing (5) with respect to d_t, which is encapsulated in ρ_t.

B. Magnetic Inductance

SWCNTs have both *magnetic* and *kinetic* inductances that can affect interconnect delay, noise, and power consumption [13, 21]. The total magnetic inductance (L_{mag}) is dependent on the entire current loop, which typically consists of a signal line and its associated ground return paths as depicted in Figure 1 [21]. Since the distribution of the current in the loop may not be known *a priori*, the concept of *partial inductance* is used to model the magnetic inductance. The partial self inductance (L_m) of a single nanotube and the mutual inductance (M_m) between two parallel current carrying nanotubes are calculated using the method described in [9]. To more efficiently model the magnetic inductance, we have developed the *equivalent conductivity model*, which approximates the magnetic inductance of the discrete SWCNTs with one conductor that has the same dimensions as the nanotube bundle [9].

The equivalent conductivity model achieved a maximum error of 6.49% with typical errors of 0.80% percent [9], which is most likely within the manufacturing tolerances of future fabrication technology. If only the self-inductance is considered [15], the magnetic inductance is significantly underestimated with typical errors of 94.3%. For sparsely packed SWCNT bundles with $P_m = 1/3$, our simulation results demonstrate that once $w_b \geq 12d_t$, the $3{\cdot}\sigma$ variation in the magnetic inductance is less than 10%. The equivalent conductivity model computes the magnetic inductance in constant time [9]. Therefore, the equivalent conductivity model provides a scalable magnetic inductance modeling solution.

C. Kinetic Inductance

In a metallic SWCNT, the kinetic inductance (L_k) is dependent on the net sum of the kinetic energy of the left and right moving electrons [13]. For individual SWCNTs, the theoretical expression for kinetic inductance is $L_k = h/(2e^2 v_F) \approx 16\ nH/\mu m$ [13]. For SWCNT bundles, the kinetic inductance is $L_{kin} = L_k/n_b$. Conflicting experimental results have been reported in the literature for the kinetic inductance of SWCNTs. In [23], kinetic inductance values of 0.1 - 4.2 $nH/\mu m$ were reported, while in [20], no kinetic inductance was observed for frequencies up to 10 GHz. Recent theoretical results indicate that when the voltage drop across the SWCNT exceeds 160 mV and l_b is significantly larger than λ_{ap}, L_k will be lower than its theoretical value [24]. Given the lack of consensus on the value of L_k, we examine its worst-case impact on future SWCNT bundle interconnect solutions in Section IV-B.

Figure 3 displays the w_b values for which the inductance of a GSG interconnect configuration experiences equal contributions from both magnetic and kinetic inductance. We assume that w_b equals the height of the bundle (h_b), $d_t = 1\ nm$, $l_b = 1\ mm$, and $P_m = 1$. Depending on the per unit length value of the kinetic inductance and the spacing between the signal bundle and the ground return bundles, the magnetic induc-

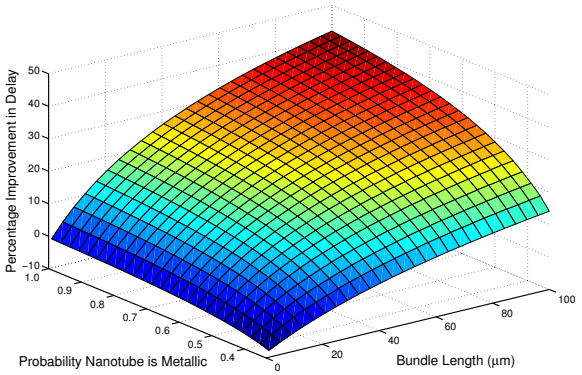

Fig. 4. Improvement in SWCNT bundle delay over copper interconnect delay for *local* interconnect.

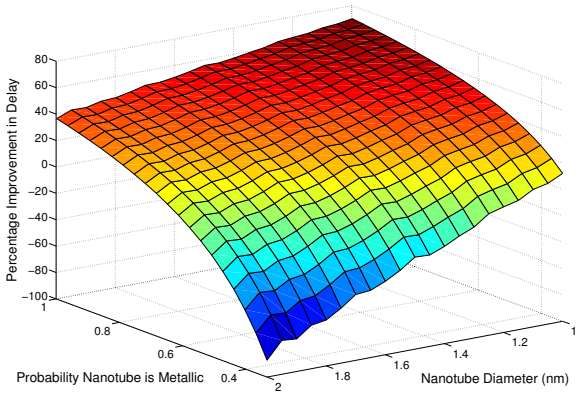

Fig. 5. Improvement in SWCNT bundle delay over copper interconnect delay for *global* interconnect.

tance dominates in bundles with w_b values ranging from 4 nm to 170 nm, which are within the range of typical width values for both local and global interconnect predicted by [2]. Therefore, the relative value of magnetic and kinetic inductance on SWCNT bundles is highly dependent on the bundle geometry, n_b, and the value of per unit length kinetic inductance.

D. Capacitance

The capacitance of a nanotube bundle consists of both a quantum capacitance (C_q) and the electrical capacitance ($C_e + C_c$). The quantum capacitance has a theoretical value of $e^2/2hv_F \approx 25\ aF/\mu m$ [13]. The electrical capacitance between adjacent nanotube bundles depends on the bundle geometry and spacing between bundles (s_b). We have developed a model for determining C_c and C_e for the geometry depicted in Figure 1. As n_b increases, the variation in capacitance values arising from the statistical distribution in nanotube locations will be reduced. To verify this assumption, we performed Monte Carlo simulations for capacitance using the interconnect analysis program FastCap [25] for different P_m values and bundle dimensions. We found that when the bundles were more than fifteen nanotubes wide, the absolute variation in the capacitance value was less than 3% for $P_m = 0.3$. This allows us to model the capacitance of the bundles by assuming a fixed placement of the nanotubes, which greatly reduces the computational resources required. We represent each bundle as a single conductor with a width of w_b and with an equivalent height of $h_{eq} = h_b(0.5 + 0.3P_m)$. The equivalent conductor's capacitance is found using the analytical model in [26]. The values of capacitance obtained using our model were compared to the results from FastCap, and the error was less than 5%.

IV. Performance and Reliability of SWCNT Bundle Interconnect

In this section, we analyze the performance and reliability of SWCNT bundles for VLSI applications using the model from Section III. To determine the delay, current density, and inductive effects arising from a particular bundle geometry, we perform HSPICE simulations on the RLC model with driver parameters and load device capacitances specified by [2].

A. Local and Global Interconnect

For local interconnect, we simulated approximately 40,000 different configurations with varying d_t, R_c, l_b, and P_m values. We use the process parameters from the 2015 node in [2]. We assume that the interconnect has a fanout of 5 gates when calculating the load capacitance, $P_m = 1/3$, $l_b = 10\ \mu m$, and $f = 10\ GHz$. The maximum current density for the simulated cases is $3.5\ \mu A$ per nanotube, which is significantly lower than the typical I_o value of $20\mu m$ [6]. Therefore, the current density in SWCNT bundles does not pose a significant performance or reliability issue. In terms of delay, the SWCNT bundle performance relative to copper interconnect primarily depends on R_{cnom}, l_b, and P_m. Figure 4 depicts the percentage improvement in SWCNT bundle delay over standard copper wires for local interconnect with $d_t = 1.5\ nm$ and $R_{cnom} = 20\ k\Omega$. For short interconnect length values, copper interconnect has less delay than SWCNT bundle interconnect due to the large contact resistance. However, the negative resistive impact of the short SWCNT bundles is offset by the effective resistance of the interconnect driver circuit. For longer interconnect, the larger SWCNT ohmic resistance leads to an improvement in delay, especially in bundles where P_m is large.

For global interconnect, we simulated approximately 1,500 different interconnect configurations with varying d_t and P_m values. We use the global interconnect process parameters from the 2015 node in [2]. We find that the current density per nanotube is similar to the values obtained for the local interconnect cases. For global SWCNT bundle delay, Figure 5 displays the percentage improvement over standard copper interconnect when $l_b = 1\ mm$, $R_c = 20\ k\Omega$, and $f = 10\ GHz$. For small d_t values, the bundle has less delay than standard copper interconnect for the full range of possible P_m values (1/3 to 1). However, for larger d_t values, P_m will determine if SWCNT bundles have less delay than copper interconnect.

B. Impact of Inductive Effects

Given the importance of inductive effects for global interconnect in standard copper technology for both performance and reliability [19], we also investigate the impact of inductance on SWCNT bundle interconnect. Inductive effects typically impact interconnect performance and reliability when

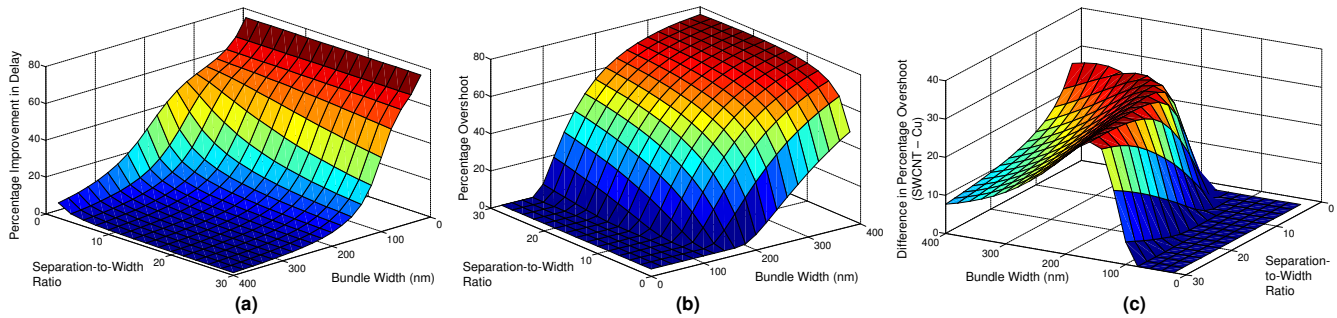

Fig. 6. The impact of inductive effects: (a) improvement in SWCNT bundle delay over copper interconnect delay; (b) voltage overshoot for SWCNT bundles; and (c) absolute difference in overshoot between SWCNT bundles and copper interconnect.

the inductive reactance (ωL) is significant compared to the resistance (R) in the system's total impedance ($Z = R + j\omega L$) [19, 27]. Figure 6a displays the percentage improvement in SWCNT bundle delay over standard copper interconnect versus w_b and the bundle separation-to-width ratio (s_b/w_b) when inductive effects are taken into account. We assume that $P_m = 1$, $d_t = 1\ nm$, $l_b = 1\ mm$, and $f = 10\ GHz$. For small w_b and s_b values, the SWCNT bundle performance improvement closely matches the improvement in resistance since $R \gg \omega L$. However, for larger w_b values, which result in decreased resistance, or larger s_b values, which result in increased inductance, the improvement in delay decreases since the inductance begins to dominate the overall resistance ($R \leq \omega L$).

Inductive effects can also cause voltage overshoot, which can damage transistors and cause logic failures [19]. Figure 6b displays the percentage voltage overshoot in SWCNT bundle interconnect. Similar to the delay behavior, the overshoot depends on the relative inductive contribution to the impedance. Since the resistance of SWCNT bundles is typically lower than that of standard copper interconnect, inductive effects impact the performance and reliability of SWCNT bundles with smaller dimensions than those of copper interconnect as depicted in Figure 6c. Therefore, it is critical that certain steps be taken in the design of SWCNT bundle interconnect systems to reduce the impact of inductive effects [19].

Understanding the relative importance of magnetic and kinetic inductance for SWCNT bundles is vital for evaluating nanotubes in VLSI interconnect applications. Figures 7a and 7b display the percentage difference in delay and voltage overshoot when modeling the total inductance and only the magnetic inductance. The addition of the worst-case theoretical kinetic inductance ($4\ \mu m/nH$) increases the delay by a maximum of 6% and voltage overshoot by a maximum of 3%. Therefore, the kinetic inductance will have a relatively small impact on SWCNT bundle performance for the interconnect geometries and process parameters predicted in [2]. The small impact of kinetic inductance stems from the difference in the behavior of $\omega L/R$ between magnetic and kinetic inductance. Since both the kinetic inductance and the resistance are inversely proportional to n_b, $\omega L_{kin}/R$ stays relatively constant (≈ 0.034 for the simulated geometry) and is not impacted by increases in s_b/w_b for a fixed w_b. In contrast, the reduced resistance due to increasing w_b and the increasing magnetic inductance due to the larger current loops generated by increasing

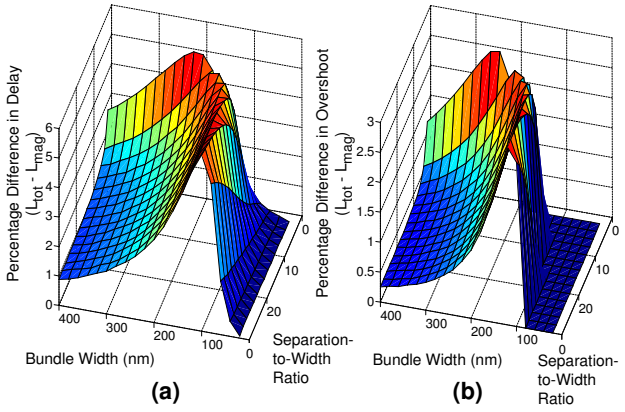

Fig. 7. The relative impact of magnetic and kinetic inductance: (a) percentage difference in delay when modeling the total inductance and only the magnetic inductance; and (b) percentage difference in voltage overshoot when modeling the total inductance and only the magnetic inductance.

s_b/w_b make $\omega L_{mag}/R \approx 1$ for many interconnect geometries. Therefore, the magnetic inductance will have a significantly larger impact on SWCNT bundle performance than kinetic inductance in predicted SWCNT bundle geometries, even when the worst-case theoretical value for L_{kin} is assumed.

C. Reliability of SWCNT Bundles

To determine the reliability impact of the statistical distribution of metallic nanotubes in global SWCNT bundles, we performed Monte Carlo simulations on 300 SWCNT bundle geometries with $10\ nm \leq w_b \leq 40\ nm$, $1\ nm \leq d_t \leq 2\ nm$, and $1/3 \leq P_m \leq 1$. We find that the delay can experience 3-sigma variations as high as 60%. Since the time required to cross large portions of the chip is significantly larger than the clock period, re-timing and buffer insertion cause the delay of many global interconnect lines to be close to the critical path delay. Figure 8 displays the probability of a timing violation on one SWCNT interconnect line for 1,000 total global SWCNT bundle interconnect lines. To ensure reasonable reliability and yield, 20 - 40 percent additional delay tolerance must be designed into systems when utilizing SWCNT bundles for global interconnect in future process technologies. However, standard copper interconnect will also experience significant variation in delay due to process variation [28]. Given the fact that SWCNT nanotube interconnect can offer up to 70%

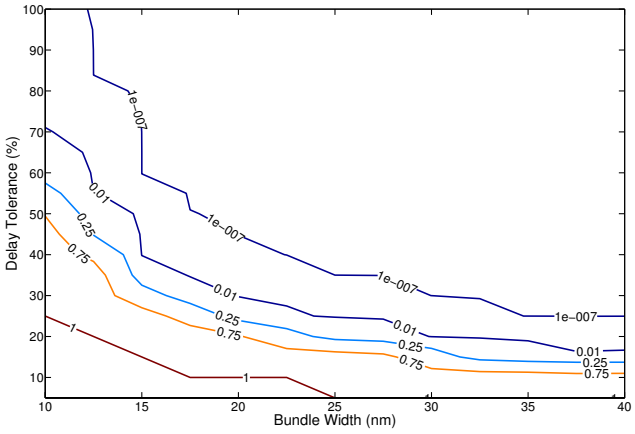

Fig. 8. Probability of a timing violation for 1,000 SWCNT bundle interconnect lines versus w_b and the additional percentage delay that the design can handle without a timing violation.

performance improvement over standard copper interconnect, SWCNT bundles offer a viable alternative to scaled copper interconnect depending on the geometric and process parameters.

V. Conclusion

In this paper, we provide a comprehensive analysis of the performance and reliability of SWCNT bundles in future VLSI applications. We develop a scalable equivalent circuit model that captures the statistical distribution of metallic nanotubes, while incorporating recent experimental and theoretical results. The results indicate that SWCNT interconnect bundles can provide significant improvement in delay over that in traditional copper interconnect. Furthermore, we demonstrate that the magnetic inductance will have a significantly larger impact on SWCNT bundle performance than kinetic inductance for predicted SWCNT bundle geometries. While many manufacturing and technological factors will ultimately contribute to the realization SWCNT bundle interconnect, the results indicate that SWCNTs have the properties to potentially be a viable replacement for copper interconnect in many high performance VLSI applications as process technology scales.

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