Approaching Speed-of-light Distortionless Communication for On-chip Interconnect

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***Abstract*— We extend the Surfliner on-chip distortionless transmission line scheme and provide more details for the implementation issues. Surfliner seeks to approach distortionless transmission by intentionally adding shunt resistors between the signal line and the ground. In theory if we distributively make the shunt conductance G=RC/L, there will be no distortion at the receiver end and the signal propagates at the speed of light. We show the feasibility and advantages of this shunt resistor scheme by a real design case of single-ended microstrip line in 0.10μm technology. The simulation results indicate we can achieve near perfect signaling of 10 Gbps data over a 10 mm serial link, yet no pre-emphasis/equalization or other special techniques are needed. Guidelines for determining the optimal value and spacing of the shunt resistors are also provided.**

I. Introduction

On-chip global interconnects have long been considered the limiting factor for high-end microprocessor design in terms of both communication latency and power consumption. Fig. 1 shows the delay trend of the global wires in MPUs based on the data from 2005 ITRS roadmap [1]. According to the prediction, the clock frequency will reach 12 GHz (or equivalently 83.3 ps cycle time) at 45 nm technology node by year 2010. At the same time, signal propagation on 1 mm global wire alone will take up to 523 ps. Note that 1 mm lines are absolutely not rare; based on Rent's rule the number of wires over 1 cm at 45 nm technology will reach 1 million. Thus we see a tremendous gap between the global interconnect performance and that required by the clock rate.

The conventional approach to tackle this "interconnect wall" is buffer insertion [2] [3]. By dividing the long interconnect into small segments, the quadratic distributive RC delay becomes linear w.r.t. the wire length. The common objectives for on-chip buffer planning are delay, power, and more recently, bandwidth [4]. However, buffer insertion is more a mitigation than a solution to the interconnect nightmare. For example, at 70 nm the optimal buffer spacing and sizing for minimum delay is 200 μm and 55x, respectively [5]. This indicates that we need a multitude of large buffers going everywhere on the chip. These large buffers not only take up a lot of active area on the substrate, but also consumes quite a fraction of power. Even worse, large number of buffers creates new problems for routing, placement and power/ground noise. Even so, the global wire delay can only be improved to 158 ps/mm with optimally planned buffers [5].

As an attractive alternative, on-chip signaling using transmission line (T-Line) has received intensive research focus in recent years. The fundamental concept behind T-Line is

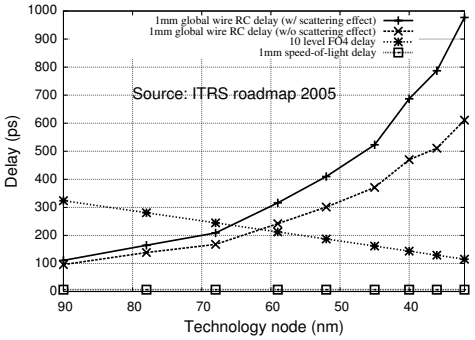

Fig. 1. Delay trend of the global interconnects.

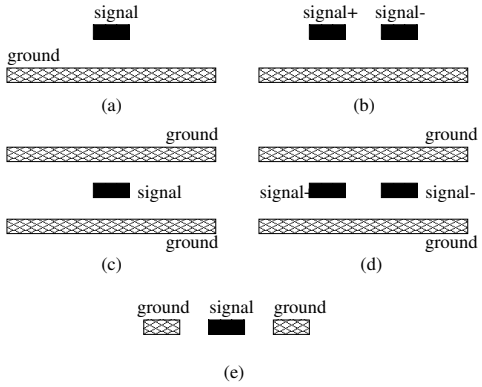

Fig. 2. Classical transmission line structures: (a) Single-ended microstrip line; (b) differential microstrip line; (c) single-ended stripline; (d) differential stripline; (e) coplanar line.

that signal propagates as an electromagnetic wave[1] rather than holistic diffusion of the electrons in the conductor. This wave behavior has a two-fold implication. First, waves are much faster than electron diffusion; they move at the speed-of-light in the dielectric. Second, wave propagation consumes much less power, because there is no need for the driver to drive the whole wire during the transmission of the symbol. The signal, once injected, leaves the driver and propagates on its own as supported by the T-Line.

Physically, T-line usually requires a larger width/spacing than RC wire with standard pitch. More importantly, to form a T-Line structure well-defined return path must be provided so as to control the inductance. For example, Fig. 2 shows some classical T-Line structures that are suitable for on-chip

[1]More specifically, signals travel in the form of TEM (Traverse Electromagnetic) for most on-chip structures with uniform cross-section.

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implementation.

In this work, we extend the Surfliner scheme for on-chip distortionless T-Line design [6] and provide simulation results in a more realistic setting. The distortionless T-Line has the unique property of enabling speed-of-light transmission with perfect signal fidelity, and Surfliner tries to mimic the behavior of distortionless T-Line by evenly adding shunt resistors.

The rest of the paper is organized as follows. In Section II, we summarize some of the previous work on on-chip T-Line modelling followed by a gentle introduction to the Surfliner scheme using shunt resistors. The theory of distortionless T-Line is then reviewed in Section III. In Section IV we use a 10 mm microstrip line case in 0.10μm to illustrate the superiority of the shunt resistor scheme. Design guidelines for optimal value and spacing of the shunt resistors are also discussed. Section V concludes the paper.

II. Previous Work

In [7] and [8], Ito et al. propose to use differential T-Line for global layer transmission, and reported measured 8 Gbps data rate under 180 nm technology. Hashimoto et al. further investigate the performance limitation of T-Lines under present and future technologies. In [9], they compare single-ended and differential T-Line against conventional buffered RC line in terms of bit rate capacity and energy, and suggested that differential T-Line is the most efficient. In [10], Akira et al. studies the tradeoff between bit rate, interconnect length and eye opening for both single-ended and differential T-Lines. More realistic situation including power/ground noise in designing T-Lines is also considered in [11].

However, typical RLC transmission line is not once for all for on-chip communication. A digital pulse with rising/falling time t_r contains wide frequency spectrum up to the knee frequency $0.35/t_r$ [3]. As we shall see in Section III, high-frequency components tend to propagate faster than low-frequency, leading to dispersion of the waveform. Meanwhile, high-frequency components experience more attenuation than low-frequency components do. The overall effect is that the shape of a digital pulse will be distorted after transmission. Thus, a leading symbol may collide with the successive symbols, causing inter-symbol interference (ISI) [12].

Various techniques were proposed to suppress the ISI effect. In [13], a pre-emphasis filter at the transmitter side was adopted to compensate for the high-frequency loss. Ron Ho et al. propose to use a clocked discharging scheme to realize time-domain equalization directly on the wire [14]. In [15] and [16], both groups of researchers propose to implement nonlinear T-Line by adding variable capacitors. The nonlinear T-Line supports solitons which can propagate with little dispersion and loss. Frequency modulation borrowed from RF communication is also attempted. In [17], a 1 Gbps data sequence is modulated onto a 7.5 Gbps carrier to ensure transmission in the LC region. Jose et al. suggest that by reducing the duty cycle of a RZ (return zero) bit piece, the frequency content of the data can be pushed more to the higher spectrum. More recently, resistive termination for T-Line has been demonstrated to be an effective way for ISI control in [18] and [19]. Both work derive analytical formula for optimal termination resistance.

In [6], Chen et al. proposed a scheme called Surfliner for implementing on-chip distortionless line. The distortionless T-Line theory requires that $RC = GL$. However, for on-chip interconnect the silicon dioxide is so good an insulator that G almost hovers about zero. Thus Surfliner explicitly add leakage resistors between the signal line and ground (or between the two signal lines in the case of differential signaling) to meet the condition.

Once the condition $RC = GL$ is met, we will show that, in Section III, all the frequency components travel at the same speed (the speed of light) so we see no dispersion. Meanwhile, all the frequency contents undergo the same amount of attenuation. The overall effect is that transmitted pulse arrives at the receiver side with perfectly preserved shape and a reduced amplitude.

In this paper, we further investigate the Surfliner scheme and discuss more implementation details. A real single-ended microstrip line case is presented to show the efficiency of the scheme. Our contribution can be summarized as follows:

- We experimentally show that, thanks to distortionless transmission, not only the ISI is highly suppressed, but also the jitter and edge rate are well-controlled. Small jitter and high edge rate at the receiver side are essential to avoid timing errors.
- By a real design case we show that the shunt resistors can be easily implemented using conventional high-resistive poly.
- We show that the distortionless T-Line is inherently a wave-pipelining scheme [20]. At the light speed (1.52E+8 m/s in S_iO_2) the time of flight (TOF) on a 20 mm global wire is roughly 131.6 ps. Assuming 10 Gbps data rate the cycle time is 100 ps, which is less than the TOF. Thus for high data rate there are multiple symbols transmitting on the wire simultaneously.
- By properly designing the wire geometry and length, we argue that termination for the distortionless T-Line is not necessary. Thus the proposed distortionless T-Line is compatible with conventional static CMOS buffers. No special transceiver circuitry is needed.
- Because the distortionless T-Line does not take full swing, and because there is no active components on the wire, the power consumption is very low. We show that, contrary to our intuition, power per bit for the distortionless T-Line actually decreases with the data rate.
- The distortionless T-Lines are robust against crosstalk and power/ground noise since it is well-shielded and no buffers are inserted.

III. Transmission Line Theory

A. The Fundamental Theory

We include the theory of transmission line [21] [6] for self-completeness of the paper. The telegrapher's equations of the transmission line is the fundamental theory behind almost all kinds of electrical interconnects, being it on-chip, packaging level or board level interconnects. Rather than lumped circuit theory, transmission line theory treats the wire as the conglomerate of numerous infinitesimal RLGC segments, one of which is shown in Fig. 3, where R, L, G, C are per unit length electrical properties defined as follows:

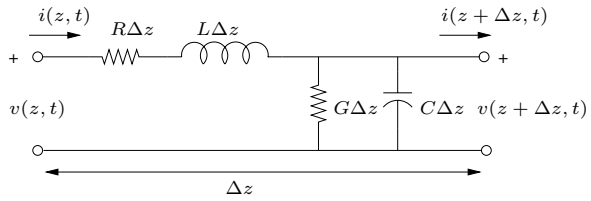

Fig. 3. RLGC model of a transmission line segment.

- R = series resistance per unit length, in Ω/m.
- L = series self loop inductance per unit length, in H/m.
- G = shunt conductance per unit length, in S/m.
- C = shunt capacitance per unit length, in F/m.

The voltage and current on the transmission line appear in the form of wave propagation; they are both functions of propagation distance z and time t, and are govern by the telegrapher's equations:

$$\frac{\partial V(z,t)}{\partial z} = -RI(z,t) - L\frac{\partial I(z,t)}{\partial t} \tag{1}$$

$$\frac{\partial I(z,t)}{\partial z} = -GV(z,t) - C\frac{\partial V(z,t)}{\partial t} \tag{2}$$

Assuming sinusoidal steady-state condition, by solving the above telegrapher's equations we can get the expression of the incident wave (which travels in the $z+$ direction):

$$V^+(z) = V_0^+ e^{-\gamma z} = V_0^+ e^{-\alpha z - j\beta z} \tag{3}$$

where

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{4}$$

is the complex propagation constant. From Eqn. (3) we see that the amplitude of the travelling wave $A(z) = V_0^+ e^{-\alpha z}$. Thus α is usually referred to as the *attenuation constant*, since 1 volt will attenuate to $e^{-\alpha}$ volt after travelling one unit distance. Similarly β is called the *phase constant*, because βz gives the phase of the voltage wave at location z. The velocity of the travelling wave is

$$v = \frac{\omega}{\beta} \tag{5}$$

The characteristic impedance of the line is defined as the ratio of voltage to current at any point of the line:

$$Z_0 = \frac{V^+(z)}{I^+(z)} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{6}$$

Note that the transmission line supports waves in both $z+$ and $z-$ directions. So the general solution to Eqn. (1) and (2) is

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{7}$$

B. Typical On-chip Transmission Line

Typical on-chip global interconnects are very lossy; The series resistance of the global interconnect is usually at the order of 10 ohm/mm. On the other hand, the silicon dioxide is a very good insulator, whose loss tangent[2] is only 0.00068. Thus for on-chip transmission line, the shunt conductance $G \approx 0$. Under these conditions, on-chip transmission line could operate in either RC region or LC region, depending on the frequency of interest.

1) RC Region: When the frequency ω is low, we have $\omega L \ll R$ and $G \approx 0$. Eqn. (4) simplifies to

$$\gamma = \alpha + j\beta = \sqrt{j\omega RC} = \sqrt{\frac{\omega RC}{2}} + j\sqrt{\frac{\omega RC}{2}} \tag{8}$$

Hence

$$\alpha = \sqrt{\frac{\omega RC}{2}} \tag{9}$$

$$v = \frac{\omega}{\beta} = \sqrt{\frac{2\omega}{RC}} \tag{10}$$

We see that in RC region, both the attenuation constant and phase velocity are functions of the frequency. More specifically, the lower the frequency, the less the attenuation, and the lower the speed. For on-chip interconnect, this $\omega L \ll R$ condition is usually satisfied in up to 10 GHz.

2) LC Region: If the frequency keeps increasing such that $\omega L \gg R$, and $G \approx 0$, then Eqn. (4) reduces to

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)j\omega C} = \frac{R}{2\sqrt{L/C}} + j\omega\sqrt{LC} \tag{11}$$

Thus

$$\alpha = \frac{R}{2\sqrt{L/C}} = \frac{R}{2Z_0} \tag{12}$$

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\epsilon_r}} \tag{13}$$

Where c_0 is the speed of light in free space and ϵ_r is the dielectric constant. We see that in the LC region, if neglecting the variation of R and L, both attenuation and phase velocity are independent of frequency. This result provides the theoretic foundation for work in [17] and [22], which seek to modulate the low-frequency content to the LC region.

C. Distortionless Transmission Line

Interestingly if we set

$$\frac{R}{G} = \frac{L}{C} \tag{14}$$

and substitute the relation in to Eqn. (4), we have

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(RC/L + j\omega C)} \tag{15}$$

$$= \frac{R}{\sqrt{L/C}} + j\omega\sqrt{LC} \tag{16}$$

Therefore

$$\alpha = \frac{R}{\sqrt{L/C}} = \frac{R}{Z_0} \tag{17}$$

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\epsilon_r}} \tag{18}$$

Likewise, plug Eqn. (14) into Eqn. (6), we have

$$Z_0 = \sqrt{\frac{L}{C}} \tag{19}$$

[2]At high frequencies, leakage currents appear in the dielectric due to the ionization of the atoms. Meanwhile, the periodic oscillation of the magnetic dipoles of the atoms also dissipates energy. These two factors contribute to the signal loss in the dielectric, and are usually indistinguishably quantified by the loss tangent (or dissipation factor) of the material.

Note in Eqn. (14) there is no assumption about ω, thus in this case we obtain frequency-independent attenuation and phase velocity across the whole spectrum. And the phase velocity is actually the speed of light in the dielectric. The characteristic impedance (Eqn. (19)) becomes pure resistive.

Eqn. (14) is usually referred to as Heaviside condition to credit Oliver Heaviside who first discovered this elegant result [23]. Based on this result Heaviside proposed to deliberately add inductance for transatlantic cable to achieve distortionless communication, and that was one hundred years ago! For on-chip application, inductance is hard to control, instead we could evenly insert leakage conductance to meet the Heaviside condition.

IV. Case Study

In this section, we use a real design case to illustrate the superiority of the distortionless T-Line. To get a better demonstration we use a single-ended microstrip line instead of a differential pair, although the latter is shown to be able to achieve higher data rate [9]. We choose 0.10 μm as the target technology, and implement the microstrip line using M7 and M9, as shown in Fig. 4. We assume the resistivity of barrier copper, ρ=2.2e-06 S/cm. The line length is 10 mm.

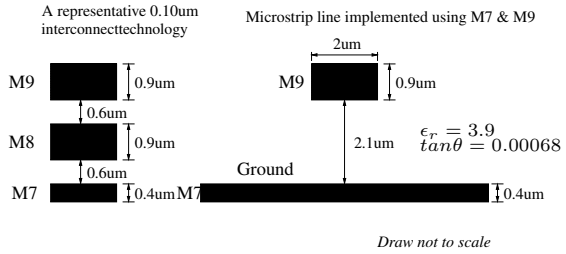

Fig. 4. A microstrip line implemented in 0.10μm technology.

A. Optimal Shunt Conductance

The first step in designing the distortionless T-Line is to determine the shunt conductance. In Eqn. (14), a hidden assumption is that RLC values of the T-Line is independent of the frequency so that we can find a single G to meet the heaviside condition. However, this is not the real scenario. For on-chip interconnect, although RLC values do not vary much, they do change over frequency. Thus a single conductance value for meeting the Heaviside condition at every frequency point is not possible. This brings up the question of what is the optimal shunt conductance.

We use a 2D EM solver called CZ2D from IBM to extract the RLGC values of the microstrip line up to 50 GHz, and the results are shown in Fig. 5. CZ2D has the capability to consider both skin-effect and proximity effect yet it is much faster than 3D extraction tools such as Raphael [24]. Clearly, as the frequency passes roughly 1 GHz, the line resistance starts to increase due to the skin-effect. Meanwhile, the total inductance decreases because the internal inductance of the line vanishes when currents rush to the surface of the conductor. The capacitance, on the other hand, is virtually constant over the whole spectrum. The leakage conductance due to the dielectric, though increases sharply at high frequencies, is still

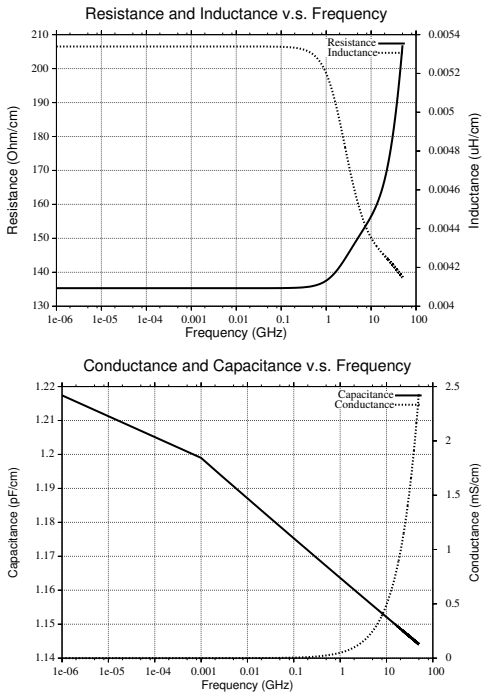

Fig. 5. RLGC values v.s. frequency for the 10 mm microstrip line.

negligible comparing to the series line resistance. The high-frequency characteristic impedance of the line is Z_0=54.9Ω, and the time of flight is 65.87 ps/cm.

As we discussed in Section III, at high frequencies the T-Line operates in the good LC region. It is in the RC region that both attenuation and phase velocity see great frequency dependency. Therefore, our rule of thumb for determining shunt conductance is "match-at-DC". Another way to understand this rule is to realize that the shunt scheme is purely passive. Rather than boosting up high-frequency components (which is not possible without active compensation/equalization), we use shunt resistors to make the low-frequency components attenuate more and travel faster.

At DC mode, we have R_{DC}=135.3Ω/cm, C_{DC}=1.22pF/cm, L_{DC}=5.34e-03μ H/cm. The total shunt resistance needed for meeting the Heaviside condition is

$$R_{\text{shunt,total}} = \frac{L_{\text{DC}}}{R_{\text{DC}} C_{\text{DC}}} = 32.41\Omega/cm. \tag{20}$$

B. Simulation Results

Assuming we evenly insert N shunt resistors for the 10 mm line, each resistor has the value

$$R_{\text{single}} = N \cdot R_{\text{shunt,total}} \tag{21}$$

In theory, we can increase N so that the line approaches a distributive distortionless T-Line. However, inserting too many shunt resistors can be prohibitive in terms of silicon resources, nor is it necessary. According to our simulation, if the spacing of the shunt resistors is less than the critical length $l_{\text{crit}} = \frac{c}{\sqrt{\epsilon_r}} \cdot t_r$, where t_r is the rising time of the signal, the transient response of the system becomes very close to that of a real distributive distortionless T-Line. If the system is targeted for 10 Gbps data transmission, the critical length l_{crit} is roughly 1.5 mm. Thus, for our 10 mm microstrip line we insert a

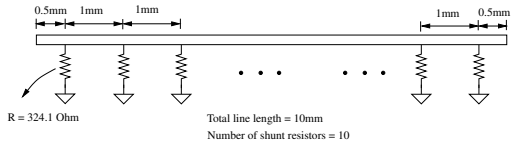

Fig. 6. On-chip implementation of the distortionless T-Line using evenly spaced shunt resistors.

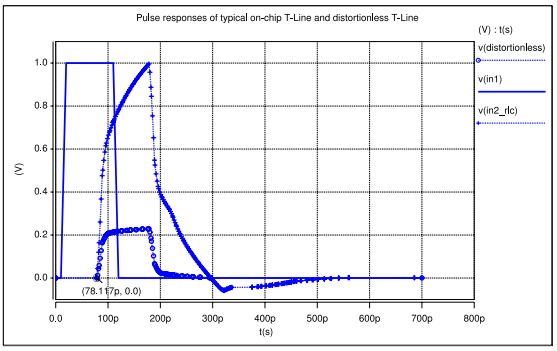

Fig. 7. Pulse responses of the 10 mm microstrip line w/o shunts and w/ 10 shunt resistors inserted (distortionless).

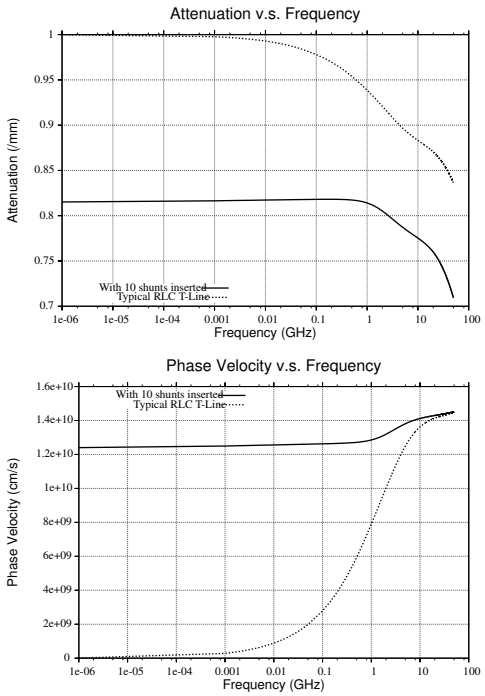

Fig. 8. Attenuation and phase velocity of the 10 mm microstrip line.

shunt resistor every 1 mm. Each shunt resistor is 324.1Ω. The design is shown in Fig. 6.

Note that a resistor of 324.1Ω can be easily implemented on-chip. For example, the sheet resistance of n^+/p^+ unsilicided polysilicon is 150∼200Ω/□ for a typical 0.25μm technology [25]. Hence the shunt scheme is completely compatible with the conventional silicon process.

Fig. 7 shows the pulse responses of the 10 mm line w/o shunts and with 10 shunt resistors inserted. The input is a trapezoidal pulse with 10 ps rising/falling time and 90 ps duration. For the typical RLC T-Line without shunts, we see both slow rising top and long tail which will lead to significant ISI. For the T-Line with 10 shunts, the pulse shape is largely preserved, but the height is reduced to approximately 0.23 volt. The DC saturation voltage, in this case, is determined by the resistance ladder formed by the series line resistance and shunt resistors. At the receiver side, a state-of-the-art sense amplifier can easily detect this amount of voltage. Both responses rise at about 78 ps, which corresponds to the time of flight of the 10 mm line.

The advantage of the shunted T-Line can also be explained in terms of the attenuation and phase velocity. Fig. 8 shows $e^{-\alpha}$ and phase velocity for both shunted T-Line and typical T-Line. We see that for shunted T-Line, the variation of attenuation over frequency is less severe than that of typical T-Line, although the overall curve is lower. More importantly, for shunted T-Line the velocity of the low-frequency components is greatly boosted up and the phase velocity curve is flat. In the case of typical RLC T-Line, the signal speed goes up from almost zero at DC and saturates at the speed of light when the frequency increases.

To evaluate the performance of the shunted T-Line, we extract the 2-port S-parameter of the 0.5mm/1mm segments using CZ2D, and then build the schematic of Fig. 6 in Hspice. Each 0.5mm/1mm wire segment is modelled using W-element with the S-parameters. The input is 1000 bit pieces of a 10 Gbps pseudo random bit sequence (PRBS). The rising/falling edges are set to be 10% of the cycle time. The eye diagram at the receiver side, as shown in Fig. 9, shows extremely clear eye opening and small jitter. Note that in this example no termination is needed for the receiver since the reflected signal attenuates to almost zero after a round trip.

Bit Rate (Gbps)	5	10	20	40
P_{avg} (mW)	2.5624	2.5754	2.6544	2.7612
E_{bit} (pJ)	0.5125	0.2575	0.1327	0.0690

TABLE I

AVERAGE POWER AND ENERGY PER BIT AT DIFFERENT BIT RATE

C. Power Consumption

A practical concern for the proposed shunted distortionless T-Line design is the static power consumption, since in this case we have direct DC path to the ground. We show that, as long as the line operates at reasonable data rate, static power consumption is rarely a problem. We measure the average power P_{avg} of 1000 bit pieces at different data rate in Hspice, and calculate the energy per bit number using the following equation:

$$E_{\text{bit}} = P_{\text{avg}} \cdot T_{\text{cycle}} \tag{22}$$

where T_{cycle} is the cycle time.

As we see from Table I, P_{avg} only increases slightly as we double the data rate. This is actually a unique property of the transmission lines. In conventional RC line, the power is used to charge and discharge the whole wire segment. In transmission lines, the energy, once injected, actually propagates down the line, and the power dissipated is due to the line loss. As we increase the data rate, P_{avg} also increases because high-frequency signals attenuate more, but not in the same ratio as the data rate increases. The energy consumed per bit, therefore, decreases for higher bit rate.

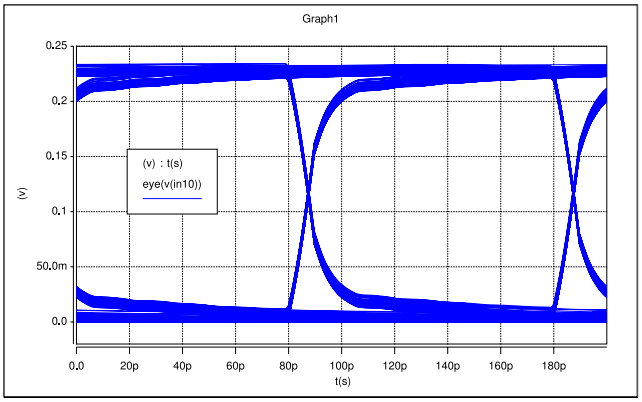

Fig. 9. Eye diagram of the 10 mm microstrip line with 10 shunt resistors inserted.

V. Conclusion

By introducing leakage resistors to meet the Heaviside condition, distortionless signaling for on-chip interconnect with speed of light is achievable. The proposed shunt resistor scheme preserves the low power property of typical transmission line, and pushed the performance to the extreme. At the time that this paper is written, a test chip in 0.35μ 1P3M technology has been fabricated and we are currently waiting for the measurement results. For future work we would like to fully exploit the potential of this new scheme for differential signaling, and consider its application in system level design.

Acknowledgment

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