A Global Minimum Clock Distribution Network Augmentation Algorithm for Guaranteed Clock Skew Yield

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Abstract— Nanometer VLSI systems demand robust clock distribution network design for increased process and operating condition variabilities. In this paper, we propose minimum clock distribution network augmentation for guaranteed skew yield. We present theoretical analysis results on an inserted link in a clock network, which scales down local skew and skew variation, but may not guarantee global skew and skew variation reduction in general. We propose a global minimum clock network augmentation algorithm, which inserts links simultaneously between all nearest sink pairs, apply rule-based link removal, and perform link consolidation by Steiner minimum tree construction for wirelength reduction with guaranteed clock skew yield. Our experimental results show that our proposed algorithm achieves dominant clock network augmentation solutions, e.g., an average of 16% **clock skew yield improvement,** 9% **maximum skew reduction, and** 25% **reduction of clock skew variation standard deviation with identical wirelength compared with previous best clock network link insertion methods [11].**

I. Introduction

The clock distribution network is one of the most critical parts in a VLSI design, significantly affects system performance and total chip power consumption. Traditional clock distribution network synthesis targets cost minimization and zero-skew realization. As VLSI system performance increases, performance margins decrease and require greater control of clock signal distribution, notably to achieve reduced clock skew. On the other hand, increasing variations in the VLSI manufacturing process and system operating conditions cause greater inter-chip and intra-chip variations, e.g., interconnect width, transistor channel length, transistor threshold voltage, supply voltage. These increased on-chip variations lead to increased clock skew variation in a chip.

The ever-increasing performance requirement and variability in a VLSI design demand new clock distribution network design techniques for robustness enhancement and improved variation tolerance. Clock skew reduction techniques include the following. (1) Insertion delay reduction. Insertion delay is the source-to-sink delay in a clock network. A reduced insertion delay is more likely associated with reduced delay and skew variation. This suggests short path lengths and large buffers in a clock distribution network. (2) Balanced / symmetric clock tree construction. Balancing a clock distribution network reduces clock skew, e.g., with an identical number of buffers in each source-to-sink path, which, at the same level, are of identical sizes and drive the same load capacitance with the same interconnect subtree topology [11]. Physical symmetry of a clock network also helps to reduce skew, e.g., in an H-tree structure.

In high-performance and high-reliability designs, clock distribution networks are implemented in symmetric non-tree structures, e.g., grids on a single dedicated routing layer. A typical high-performance/reliability clock distribution network includes three levels: (1) a symmetric tree at the top level; (2) a grid; and (3) Steiner trees which connect clock pins of each sequential element to the clock distribution grid. Such a clock network achieves reduced clock skew and improved process variation robustness at the cost of routing resource and power consumption.

Recent methodologies have migrated high-performance clock distribution network design techniques to ASIC designs. For example, including extra routing in a clock tree is proposed as an effective technique for clock skew and skew variation reduction in an ASIC design with minimum wirelength increase. Several clock network augmentation approaches are as follow. Link insertion based on simple heuristic rules and minimum weighted matching is proposed in [8], and improved in [9]. An inserted link brings (1) extra resistive connection, and (2) extra interconnect capacitance to a clock network. The authors of [8] proposed to adjust clock routing to restore capacitance balance in a clock network after link insertion, and restrict link insertion between nodes with zero nominal skew, which does not affect the delay to any other node in the clock network. An iterative link insertion scheme based on statistical skew variation analysis was presented in [2]. This method is guided by more accurate skew and skew variation analysis, and applies rank-one update for matrix inverses for efficiency improvement of iterative skew variation analysis. The authors propose to include dummy capacitance to restore capacitance balance in a clock network after link insertion. For more practical application, e.g., in a buffered multi-level clock network, techniques have been proposed to address practical issues, e.g., to avoid the multi-driver interconnect problem introduced by link insertion by proposed design criteria [11].

In this paper, our contributions are as follows.

- We formulate the clock skew reduction problem as a parametric yield optimization problem, based on statistical

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analysis in an on-chip variation model. We propose minimum clock network augmentation for guaranteed skew yield, i.e., to reduce wirelength in an augmented clock network while guaranteeing the probability for the global skew of the clock network to meet the required skew bound.

- We present theoretical results for iterative link insertion in an RC interconnect. We prove that a purely resistive link in an unbuffered RC clock network scales down local skew between the two nodes by a ratio of $\frac{r}{r+\gamma}$, and scales down the driver admittance difference of the two nodes by the same ratio in a buffered RC clock network. In general, an inserted link does not guarantee global skew and skew variation reduction in an RC clock network.
- We propose minimum clock network augmentation for guaranteed skew yield, which comprises three steps: (1) simultaneous link insertion between nearest sink pairs in a clock network, (2) rule-based link removal with guaranteed clock skew yield, and (3) link consolidation by Steiner minimum tree construction for further wirelength reduction.
- We validate our proposed method with SPICE-based Monte Carlo simulations considering spatially correlated variations. Our experimental results show that our proposed algorithm achieves substantially dominatin solutions compared with previous best clock network link insertion methods [11].

The remainder of the paper is organized as follows. We present existing on-chip variation models and clock network link insertion methods in Section II, and give our problem formulation in Section III. We present our theoretical analysis results in Section IV, and propose our mesh-reduction-based novel clock network augmentation method in Section V. We present our experimental results in Section VI, and conclude in Section VII.

II. OCV and Previous Link Insertion Methods

A. On-Chip Variation

Technology advancement in VLSI manufacturing enables continuous aggressive scaling of transistor and interconnect dimension, which results in an ever increasing number of components integrated in a single chip and continuous system performance improvement. On the other hand, the latest VLSI manufacturing process technologies also introduce increased variabilities of process and environmental parameters. As a result, modern VLSI design and analysis tools take into consideration both inter-chip and intra-chip variations. The inter-chip variations are the same for all components in a chip. The intra-chip variations represent variability between components in a chip, and include spatially correlated variations, and purely uncorrelated variations. Therefore, a process / design parameter p can be decomposed into its nominal value p_0, global or inter-chip variation ε_1, spatially correlated variation ε_2, and purely uncorrelated variation ε_3 as follows.

$$p = p_0 + \varepsilon_1 + \varepsilon_2 + \varepsilon_3 \tag{1}$$

Pelgrom [7] proposed a spatial correlation model in 1998, which characterizes the difference of a parameter of two devices in a chip by its standard deviation, as follows.

$$\sigma_p^2 = \frac{A_p}{WL} + S_p^2 D^2 \tag{2}$$

where W and L are respectively transistor channel width and length of the two devices, D is the distance between the two devices, A_p and S_p are coefficients.

A latest spatial correlation model is proposed in [3], which observes a linear relationship between the distance x of two devices, and the correlation ρ of a parameter of the two devices, as follows.

$$\rho = \begin{cases} 1 - \frac{x}{X_L}(1-\rho_B) & (x \le X_L) \\ \rho_B & x > X_L \end{cases} \tag{3}$$

where the correlation becomes ρ_B if the two devices are more than X_L distance apart.

B. Previous Link Insertion Methods

Previous clock network link insertion methods identify the candidate pairs with tree-topology based algorithms [11] or nominal delay based rules [8]. Three heuristic criteria ("rules") [9] are proposed for selecting a pair of nodes in a clock network for creation and insertion of a new link:

1. small resistance $\alpha = \frac{R_l}{R_{loop}} \le \alpha_{max}$,
2. small capacitance $\beta = \mid \frac{C_l}{2}(R_{u,u} - R_{w,w}) \mid \le \beta_{max}$, and
3. small depth of common ancestor node γ [9].

A fourth rule is proposed to avoid repeated link insertions between two subtrees [11]. These heuristic rules provide very efficient optimization algorithms, and are moreover extended in [11] to statistical clock skew reduction under process variation.

A more accurately guided and less efficient link insertion scheme is proposed in [2]. This method applies greedy iterative link insertion in a clock network based on statistical clock skew variation analysis on a first order variation model. The Elmore delay, i.e., the $G^{-1}C$ matrix of the clock network, is updated incrementally during each link insertion. A rank-one update method is applied for better efficiency, which updates matrix inverse in $O(mnx)$ time, where m is the number of random variables, n is the number of nodes, x is the number of inserted links.

In summary, previous works have the following limitations. (1) Clock skew yield is not guaranteed. (2) They do not consider link removal. (3) Rules based on nominal delay in the orignial clock routing tree may not accurately reflect the augmented clock network and guide the link insertion procedure to achieve the optimum augmentation. Our work addresses all three of these limitations.

III. Minimum Clock Network Augmentation for Guaranteed Skew Yield

We consider a clock distribution network as an RC interconnect, where the resistance and the capacitance for an intercon-

nect segment (i, j) of length l and width w are given by

$$\begin{aligned} r_{ij} &= r\frac{l}{w} \\ c_{ij} &= cwl \end{aligned} \quad (4)$$

where r and c are unit square resistance and unit square capacitance of interconnect respectively.

We take into account the following significant on-chip variations for clock network analysis and optimization in this paper (as in [11]).

1. Interconnect variation, e.g., in width, height, and interlayer dielectric thickness, which results in interconnect resistance and capacitance variations.
2. Sink capacitance variation, which comes from variation of gate capacitance of the receiver transistors of an interconnect.
3. Transistor channel length variation, which affects driving strength of the buffers in a clock network.
4. Supply voltage drop variation, which leads to timing degradation for the buffers in a clock network.

We consider global, spatially correlated, and uncorrelated components for each variation, and follow the spatial correlation rule (3) observed in [3].

We define *clock skew yield*, Y_s, as the probability that the clock skew is within the clock skew bound, i.e.,

$$Y_s = P(s < U) \quad (5)$$

We now formulate the *guaranteed skew yield minimum clock network augmentation problem* as follows.[1]

Problem 1 (Minimum Clock Network Augmentation) *Given*

1. *a clock distribution interconnect network N,*
2. *clock network sinks K,*
3. *clock buffers B,*
4. *interconnect unit square resistance r,*
5. *interconnect unit square capacitance c,*
6. *interconnect width w_{ij} for interconnect segment $(i, j) \in N$, its mean $\mu(w_{ij})$, variance $\sigma^2(w_{ij})$ and correlation $\rho(w_{ij}, w_{lk})$ between interconnect segments (i, j) and (l, k),*
7. *sink capacitance c_k for each sink $k \in K$, its mean $\mu(c_k)$, variance $\sigma^2(c_k)$ and correlation $\rho(c_k, c_l)$ between sinks k and l,*
8. *gate length L_b^g for each buffer $b \in B$, its mean $\mu(L_b^g)$, variance $\sigma^2(L_b^g)$ and correlation $\rho(L_{b1}^g, L_{b2}^g)$ between gates b_1 and b_2,*
9. *supply voltage V_b^{dd} for each buffer $b \in B$, its mean $\mu(V_b^{dd})$, variance $\sigma^2(V_b^{dd})$ and correlation $\rho(V_{b1}^{dd}, V_{b2}^{dd})$ between two gates b_1 and b_2,*
10. *clock skew upper bound U,*
11. *required skew yield Y_s,*

find an augmented clock network N' with minimum wirelength which guarantees the required skew yield Y_s.

[1] A more generalized problem formulation is independent of the extraction and on-chip variation models that we present here (which are consistent with those of the previous methods), and our proposed method can also be extended to be applied to more advanced extraction and on-chip variation models.

IV. Theoretical Analysis

A. Local Skew

In this section, we derive theoretical results for the effect of an inserted link in an RC clock distribution network on local skew (variation), i.e., the skew (variation) between the two nodes which the inserted link connects.

In an RC clock network, we define the conductance matrix $G_{n\times n}$, where n is the number of nodes in the clock network excluding the clock source s, $G_{ij} = -\frac{1}{r_{ij}}$ is the negative reciprocal of the resistance between two nodes i and j, and $G_{ii} = \sum_{j\neq i} \frac{1}{r_{ij}} + \frac{1}{r_{is}}$ includes all resistance between node i and its neighbors j, including the resistance r_{is} between node i and the clock source s. We define the capacitance matrix $C_{n\times n}$, where $C_{ii} = c_i$ is the ground capacitance of node i, $C_{ij} = 0, i \neq j$.

The Elmore delays from the clock source s to the sinks are given by a $n \times 1$ vector $D^E_{n\times 1} = G^{-1}CI$, where I is a $n \times 1$ unit vector, $I_i = 1, \forall 1 \leq i \leq n$. Higher order, e.g., p-th order moments of the delays are given by $(G^{-1}C)^p I$ [6].

Theorem 1 *Inserting a purely resistive link in an unbuffered RC clock network scales down the skew and the skew variation between the two nodes, e.g., by a ratio of $\frac{r}{r+\gamma}$, where r is the inserted link resistance, $\gamma = G_{ii}^{-1} + G_{jj}^{-1} - 2G_{ij}^{-1}$.*

Proof. Inserting a resistive link r between nodes i and j updates the conductance matrix G by

$$G' = G + gVV^T \quad (6)$$

where $g = \frac{1}{r}$, V is a $n \times 1$ vector, $V_i = 1$, $V_j = -1$, $V_{k\neq i,j} = 0$, V^T is transpose of vector V.

Applying the rank-one update for matrix inverses [5, 4] gives

$$(G + gVV^T)^{-1} = G^{-1} + \beta G^{-1}VV^TG^{-1} \quad (7)$$

where

$$\begin{aligned} \beta &= -\frac{1}{r+\gamma} \\ \gamma &= V^TG^{-1}V = G_{ii}^{-1} + G_{jj}^{-1} - 2G_{ij}^{-1} \end{aligned} \quad (8)$$

An entry in $G^{-1}VV^TG^{-1}$ is given by

$$(G^{-1}VV^TG^{-1})_{kl} = (G_{ik}^{-1} - G_{jk}^{-1})(G_{il}^{-1} - G_{jl}^{-1}) \quad (9)$$

We have the local skew between nodes m and n as follows.

$$\begin{aligned} &(G'^{-1}CI)_m - (G'^{-1}CI)_n = \sum_q ((G_{mq}^{-1} - G_{nq}^{-1}) \\ &+ \quad \beta(G_{im}^{-1} - G_{jm}^{-1} - G_{in}^{-1} + G_{jn}^{-1})(G_{iq}^{-1} - G_{jq}^{-1}))C_q \end{aligned} \quad (10)$$

For $m = i, n = j$, this gives

$$\begin{aligned} &(G'^{-1}CI)_i - (G'^{-1}CI)_j \\ &= \sum_q (1 + \beta\gamma)(G_{iq}^{-1} - G_{jq}^{-1})C_q \\ &= \frac{r}{r+\gamma}((G^{-1}CI)_i - (G^{-1}CI)_j) \end{aligned} \quad (11)$$

Higher order moments follow the same scaling ratio.

$$\begin{aligned} & ((G'^{-1}C)^p I)_i - ((G'^{-1}C)^p I)_j \\ = & \sum_q (1+\beta\gamma)((G_{iq}^{-1})^p - (G_{jq}^{-1})^p) C_q \\ = & \frac{r}{r+\gamma}(((G^{-1}C)^p I)_i - ((G^{-1}C)^p I)_j) \end{aligned} \quad (12)$$

Therefore, inserting a purely resistive link r scales local skew and local skew variation by a ratio of $\frac{r}{r+\gamma}$. □

This ratio of $\frac{r}{r+\gamma}$ is consistent with previous results. E.g., in a tree structure clock network, G_{ii}^{-1} is the resistance of the path from source s to sink i, G_{jj}^{-1} is the resistance of the path from source s to sink j, and G_{ij}^{-1} is the common path resistance of sinks i and j. In [9], the first heuristic rule is based on the ratio of the link resistance and the resistance of the loop which is formed by the link.

Following the same line of derivation, we have the following theorem on the effect of an inserted purely resistive link on the scaling of the driver admittance moments, which are given by $G^{-1}B$, $G^{-1}CG^{-1}B$, ...$(G^{-1}C)^pG^{-1}B$, respectively, where B is a $n \times 1$ vector, $B_i = 1$ if node i is a driver, $B_i = 0$ otherwise [6].

Theorem 2 *Inserting a purely resistive link between two nodes with different drivers in a buffered RC clock network scales down the difference of the driver admittance moments by a ratio of $\frac{r}{r+\gamma}$, where r is the inserted link resistance, $\gamma = G_{ii}^{-1} + G_{jj}^{-1} - 2G_{ij}^{-1}$.*

Proof. Omitted due to space limitation. □

The scaling ratio of the driver gate delay difference may differ due to the non-linearity between gate delay and driver admittance.

B. Global Skew

As we present in the previous section, link insertion in an RC clock network is an effective technique to reduce local skew and local skew variation. In this section, we study the effect of an inserted link on global skew (variation), i.e., the maximum skew (variation) between two nodes in a clock distribution network. We observe that an inserted link in a clock network has two effects: (1) resistive connection between the two nodes, and (2) updated capacitance balance in the network.

The augmented (1) resistive connection helps to reduce local skew and local skew variation between two nodes (Theorem 1), but, in general, does not guarantee global skew or skew variation reduction. One reason is the global effect, e.g., an inserted purely resistive link between a maximum delay node i and a minimum delay node j reduces the delay to node i, which may also reduce the delay to an upstream node k in the path between the clock source s and node i. When node k is a second minimum delay node, e.g., with a delay of $d_{min} + \delta$, this link insertion may increase the global clock skew. However, this scenario is less likely to occur in a balanced clock distribution network, where clock sinks have equal depth.

The other more common reason for an inserted link not to guarantee skew and skew variation reduction is the (2) updated capacitance balance effect. E.g., an inserted link increases the capacitance at the two sinks and increases the delay to the two sinks, which alters the skew between each of the two nodes and any other sink in the clock network. This capacitive effect of an inserted link suggests a global optimization of the problem, i.e., a local / partial link insertion cannot guarantee global capacitance balancing and minimized global skew. An iterative link insertion procedure may not have monotone clock skew (variation) reduction in achieving the minimum skew (variation), i.e., there may not exist an iterative link insertion procedure with monotone clock skew reduction which achieves the minimum skew (variation).

We propose a "batched" link insertion scheme, e.g., to insert a large number of links at the same time for guaranteed clock skew yield, and proceed with a post-processing procedure to reduce wirelength by link removal. We base link removal procedure on the analysis result of the skew yield of the augmented clock network, which gives more accurate analysis results for the final augmented clock network.

V. Optimization Algorithm

Based on the analyses of the preceding section, we propose a new clock distribution network augmentation algorithm for wirelength reduction with guaranteed clock skew yield. Our proposed algorithm (see the Algorithm 1 template) has three main steps:

1. Link insertion between all pairs of sinks which are within a short distance ε for guaranteed clock skew yield, as is suggested by Theorems 1 and 2, e.g., to insert links of small resistances.
2. Link removal based on statistical yield analysis (e.g., SPICE Monte Carlo simulation) and two heuristic rules, for wirelength minimization with minimum skew yield compromise.
3. Link consolidation by replacing minimum spanning trees with Steiner minimum trees for further wirelength reduction. The runtime of the proposed algorithm is dominated by statistical clock network analysis.

The proposed Algorithm 1 approach has three major advantages.

- *Smooth optimization.* Iterative link insertion starting with a tree structure may not observe monotone global skew reduction, e.g., due to the updated capacitance balance effect of the inserted links. Removing links from a mesh structure clock network leads to more easy control of the optimization process, e.g., with minimum clock skew yield compromise.
- *Accurate analysis.* We remove links based on the statistical analysis result for the skew variation in the augmented clock network (after step (1) link insertion), which is very close to the final augmented clock network (after step (3)), and is much more accurate than the previous methods which insert links based on the nominal delay analysis in the original clock tree.
- *Ease of physical routing of the clock links.* In our algorithm, we include all (shortest) links at the same time.

Clock links are evenly distributed in the layout plane with minimum wirelength, with possible routing obstacle consideration. There is no hassle of rip-up and re-route as in an iterative clock link insertion scheme.

Algorithm 1:
Clock Network Augmentation for Guaranteed Skew Yield

Input: Clock Distribution Network N, buffers B, sinks S, unit square interconnect resistance r, capacitance c, wire width w, sink capacitance C_k, gate length L^g supply voltage V^{dd}, and their variabilities

Output: Augmented Clock Distribution Network N'

1. Link insertion between all pairs of sinks within a distance ε
2. Statistical clock skew analysis
3. Rule based link removal
4. Iterative link removal
5. Link consolidation by Steiner tree construction
6. Final statistical skew yield evaluation

We give a detailed description for each procedure in our algorithm in the following subsections.

A. Mesh Formation

Based on the analysis results and the observations in the previous section, e.g., a single inserted link may not guarantee global skew (variation) reduction, we propose to insert a sufficiently large number of links at the same time in a clock distribution network for guaranteed skew yield. We prefer to insert shortest links, because (1) limited routing resource imposes wirelength constraints, and (2) shortest links imply minimum capacitance balance update, which is largely responsible for the complexity of the problem.

We insert links between all pairs of sinks which are within a distance of ε, and obtain a mesh-like clock network structure. We guarantee the required clock skew yield while leaving enough room for mesh reduction optimization by tuning the distance threshold ε, e.g., a larger ε gives a larger wirelength and a smaller clock skew.

B. Mesh Reduction

We perform statistical clock skew analysis on the augmented clock network, e.g., by applying SPICE Monte Carlo simulation, and reduce wirelength by selectively removing part of the inserted links. For efficiency, we establish the following two rules.

Definition 1 *A maximum delay sink is a sink which has the maximum delay in the clock network in at least one of Monte Carlo SPICE simulation runs.*

Definition 2 *The maximum skew between two sinks is the maximum delay difference in all of the Monte Carlo SPICE simulation runs.*

Definition 3 *A comparable delay sink pair are two sinks of which maximum skew is smaller than a threshold* α.

Rule 1 *Remove links between two "maximum delay sinks".*

Rule 2 *Remove links between a "comparable delay sink pair".*

Removing a purely resistive link between two nodes with identical (comparable) delays have no (minimum) impact on the local and the global skew of the clock network. Removing a link between two maximum delay sinks reduces the capacitances at the two sinks and helps to reduce the global clock skew.

We apply Rule 1 to remove all links between two maximum delay sinks, and apply Rule 2 to remove all links with their maximum skew less than α, which is a pre-defined maximum skew threshold such that link removal would not compromise the clock skew yield. We proceed to apply optional iterative link removal, e.g., to gradually increase α or to remove links in an increasing order of the maximum skew between the sinks for further wirelength reduction without skew yield compromise (Algorithm 1). In iterative link removal, we need to verify clock skew yield at each link removal. The runtime of this procedure is dominated by statistical clock skew analysis.

C. Link Consolidation

The inserted links form spanning trees. It is possible to further reduce wirelength by constructing Steiner minimum trees (SMTs) in place of spanning trees. We cluster sinks which are connected by links, and links which have overlapped bounding boxes. For efficient computation of link bounding box overlaps, we apply a line-scanning algorithm, which sorts the link bounding boxes by their x coordinates in an array X, sweeps the layout plane in x direction, keep an array Y of link bounding boxes which intersect with the scanline, sort the array based on their y coordinates, and identify overlaps by going along the scanline in y direction and finding an array A of active link bounding boxes. This line-scanning algorithm takes $O(n \log n)$ time, where n is the number of links. We construct Steiner minimum trees for each cluster of sinks by applying the GeoSteiner 3.1 package [13]. Algorithm 2 summarizes our link consolidation method.

Algorithm 2: Link Consolidation Algorithm

Input: Spanning trees $\{T\}$ of inserted links over sinks S

Output: Steiner Minimum trees $\{T'\}$ over sinks S

1. For each link (i, j)
2. Cluster i and j
3. Sort link endpoints by their x coordinates in an array X
4. Sweep scanline over the layout plane, stop at each $x_{sl} \in X$
5. If link (i, j)'s left endpoint i has x coordinate $x_i = x_{sl}$
6. Insert link endpoints i and j into an array Y
7. Update sorting of array Y by y coordinates
8. If link (i, j)'s right endpoint j has x coordinate $x_j = x_{sl}$
9. Remove link endpoints i and j from array Y
10. For each endpoint $i \in Y$
11. If i is bottom endpoint of link (i, j)
12. Insert link endpoints i and j into array of active links A
13. Link (i, j)'s bbox overlaps with those of active links in A
14. Cluster i and j with link endpoints in array A
15. If i is top endpoint of link (i, j)
16. Remove link endpoints i and j from array A
17. Construct Steiner minimum trees $\{T'\}$ for each cluster of sinks

TABLE I
TESTCASE PROPERTIES.

Case	#Sinks	Delay(ps)	Skew(ps)	WL (μm)	Total cap(pF)
s9234	135	367	0.5	37043	6.44
s5378	164	379	2.9	42522	7.41
s13207	500	662	11.7	129203	23.01

VI. EXPERIMENTS

In the following experiments, we apply our proposed algorithm for minimum augmented clock networks, and compare with the initial tree structure clock networks, and augmented clock networks achieved by the state-of-art link insertion method [11].

As in [11], we conduct our experiment on the ISCAS89 benchmark suite. A mapped netlist is synthesized with SIS [10] and the circuit placement is obtained with an academic placement tool *mPL* [12]. Assuming a 180*nm* technology with parameters from [1], wire capacitances are extracted by SPACE 3D [14]. Table I gives the properties of the balanced clock routing trees. We consider 5% standard deviations for the variations of interconnect width, sink capacitance, transistor channel length, and supply voltage. We consider spatial correlations (3) which degrade linearly as the distance between the two components increases.

Our proposed method is implemented in C++ and runs on an Intel Xeon 2.4GHz system. For each statistical clock network analysis, we apply 1000 HSPICE Monte Carlo simulation runs, and report skew yield (**SY**), maximum skew (**MS**) and standard deviation (**SD**) of skew variations. We compare improvements for each step of our proposed algorithm, and compare our proposed method with one of the best previous methods [11].

We gradually increase threshold distance ε in mesh formation and obtain the wirelength and skew yield tradeoff curve. Figure 1 presents wirelength increases with different skew yields for testcase "s13207". The skew yield increases rapidly with the first few short links. However, more and longer links are needed to improve skew yield when the skew yield is close to 100%. Figure 2 shows wirelength increases with different skew bounds for 100% skew yield for testcase "s13207". The skew bound varies from 50*ps* to 110*ps*. Smaller clock skew bounds lead to increased wirelength of the clock distribution network, e.g, towards to a mesh structure. Figures 1 and 2 show two aspects of the same wirelength increase trend. The 100% skew yield point in Figure 1 corresponds to the 100*ps* skew bound point in Figure 2.

Table II presents improvement and runtime for each step of our proposed method. The wirelength, maximum skew, standard deviation results are normalized by those of the initial balanced trees. As in [11], the skew bounds of the three testcases are 50ps, 50ps and 100ps, respectively. We choose maximum skew threshold value α (in Rule 2) as 2% skew bound. Skew yield requirement is 100%. We observe that link removal significantly reduces clock network wirelength, e.g., by an average of 68% for these test cases, with slightly increased maximum skew and standard deviation and uncompromised skew yield. Link consolidation further reduces an average of 25% wirelength for these testcases without increasing maximum skew and standard deviation. The runtime in Table II is dominated by statistical clock network analysis, e.g., in 100 HSPICE simulation runs.

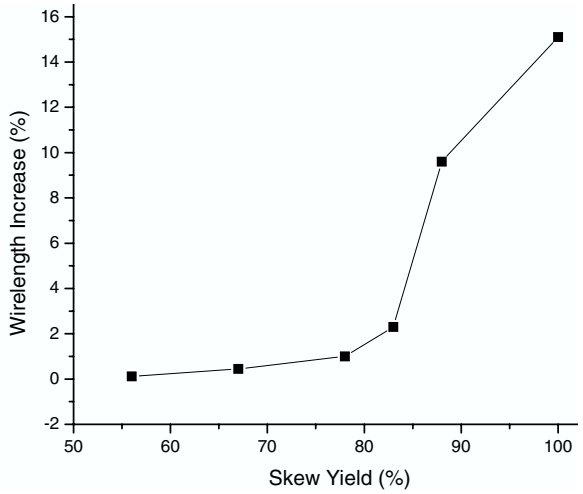

Fig. 1. Wirelength increases with different skew yields with 100*ps* skew bound for testcase "s13207".

Table III compares our proposed method with one of the best existing method [11], e.g., with identical clock network wirelength bound. We observe that our proposed algorithm achieves dominant results than the existing method in terms of skew yield, maximum skew and standard deviation. E.g., our method achieves an average of 16% clock skew yield improvement, 9% maximum skew reduction, and 25% reduction of clock skew variation standard deviation with identical wirelength for these test cases.

VII. CONCLUSION

In this paper, we formulate the clock distribution network augmentation problem as a statistical optimization problem, i.e., to achieve guaranteed clock skew yield with minimum wirelength increase. We present theoretical analysis on the effect of an inserted link, which scales down the local skew and skew variation between the two sinks by a ratio of $\frac{r}{r+\gamma}$, and the driver admittance difference of the two sinks by the same ratio. In general, an inserted link does not guarantee global skew and skew reduction in a clock distribution network. We propose a global minimum clock distribution network augmentation algorithm for guaranteed clock skew yield, which augments a clock network by including all shortest links between sinks for required clock skew yield, and reduces wirelength by selective removing of the inserted links based on statistical skew analysis on the augmented clock network. We finalize the clock network augmentation by constructing Steiner minimum trees in place of the spanning trees which are formed by the inserted links.

Our experimental results show that our proposed algorithm achieves dominant clock network solutions. For example, we achieve an average of 16% clock skew yield improvement, 9% maximum skew reduction, and 25% reduction of clock skew variation standard deviation with identical wirelength com-

TABLE II

SKEW YIELD (SY), WIRELENGTH(WL), MAXIMUM SKEW (MS) AND STANDARD DEVIATION OF SKEW VARIATION (SD) (NORMALIZED BY THOSE OF INTIAL CLOCK TREES) WITH 100% SKEW YIELD OF (1) INITIAL CLOCK TREES, (2) CLOCK MESHES, (3) REDUCED CLOCK MESHES, AND (4) CONSOLIDATED AND REDUCED CLOCK MESHES.

	Initial Tree				Mesh					Mesh + deletion					Mesh + deletion + consolidation				
Testcases	SY	WL	MS	SD	SY	WL	MS	SD	CPU(s)	SY	WL	MS	SD	CPU(s)	SY	WL	MS	SD	CPU(s)
s9234	0.42	1	1	1	1.00	2.18	0.55	0.55	0.00	1.00	1.37	0.59	0.74	3.66	1.00	1.26	0.59	0.74	3.67
s5378	0.38	1	1	1	1.00	1.96	0.55	0.66	0.01	1.00	1.28	0.56	0.71	4.04	1.00	1.21	0.56	0.71	4.05
s13207	0.48	1	1	1	1.00	1.54	0.74	0.69	0.02	1.00	1.19	0.74	0.86	10.95	1.00	1.15	0.74	0.86	10.96
Normalized Avg	1	1	1	1	2.34	1.89	0.61	0.63	0.01	2.34	1.28	0.63	0.77	6.22	2.34	1.21	0.63	0.77	6.23

TABLE III

SKEW YIELD (SY), WIRELENGTH(WL) (NORMALIZED BY THAT OF INITIAL CLOCK TREES), MAXIMUM SKEW (MS) (*ps*) AND STANDARD DEVIATION OF SKEW VARIATION (SD) (*ps*) OF CLOCK NETWORKS ACHIEVED BY (1) LINK INSERTION METHOD IN [11], AND (2) OUR PROPOSED METHOD WITH IDENTICAL CLOCK NETWORK WIRELENGTH.

	[11]				Ours			
Testcases	SY	WL	MS(*ps*)	SD(*ps*)	SY	WL	MS(*ps*)	SD(*ps*)
s9234	0.95	1.08	64	10	0.99	1.08	56	8
s5378	0.63	1.01	94	14	0.79	1.01	79	11
s13207	0.61	1.01	180	27	0.76	1.01	174	19
Normalized Avg	1	1	1	1	1.16	1	0.91	0.75

pared with one of the best previous clock network link insertion methods [11].

Our ongoing research efforts include efficiency improvement via statistical delay calculation, and link insertion across buffers in a clock distribution network.

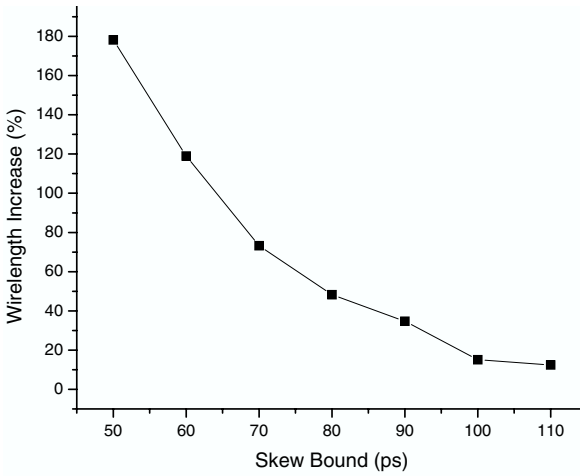

Fig. 2. Wirelength increases with different skew bounds with 100% skew yield for testcase "s13207".

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[12] CPMO-constrained placement by multilevel optimization. `http://ballade.cs.ucla.edu/cpmo/`.

[13] GeoSteiner: Software for Computing Steiner Trees. `http://www.diku.dk/geosteiner/`.

[14] SPACE: VLSI physical design modeling and verification. `http://space.tudelft.nl`.