Coupling-aware Dummy Metal Insertion for Lithography *

Liang Deng, Martin D. F. Wong
Dept. of Electrical & Computer Engineering
University of Illinois at Urbana-Champaign
{ldeng,mdfwong}@uiuc.edu

Kai-Yuan Chao
Intel Corporation
Hillsboro, OR
kaiyuan.chao@intel.com

Hua Xiang
IBM TJ Watson Research Center
Yorktown, NY
huaxiang@us.ibm.com

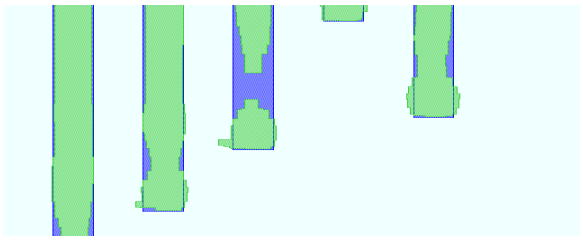
Abstract— As integrated circuits manufacturing technology is advancing into 65nm and 45nm nodes, extensive resolution enhancement techniques (RETs) are needed to correctly manufacture a chip design. The widely used RET called off-axis illumination (OAI) introduces forbidden pitches which lead to very complex design rules. It has been observed that imposing uniformity on layout designs can substantially improve printability under OAI. For metal layers, uniformity can be achieved simply by inserting dummy metal wire segments at all free spaces. Simulation results indeed show significant improvement in printability with such a dummy metal insertion approach. To minimize mask cost, it is advantageous to use dummy metal segments that are of the same size as regular metal wires due to their simple geometry. But these dummy wires are printable and hence increase coupling capacitances and potentially affect yield. The alternative is to use a set of parallel sub-resolution thin wires (which will not be printed) to replace a printable dummy wire segment. These invisible dummy metal segments do not increase coupling capacitances but bring a higher lithography cost, which includes mask cost and RET/process expense. This paper presents a strategy for dummy metal insertion that can optimally trade off lithography cost and coupling capacitance. In particular, we present an optimal algorithm that can minimize lithography cost subject to any given coupling capacitance bound. Moreover, this dummy metal insertion will achieve a highly uniform density because of the locality of coupling capacitance, which automatically ameliorates chemical mechanical polish (CMP) problem.

I. Introduction

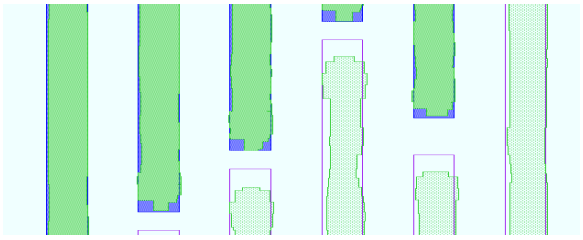
The continuing CMOS technology scaling down has pushed the integrated circuits manufacturing to a limit. Photolithography becomes a main issue related to process variations and yield problems. Resolution enhancement techniques (RETs) have been used extensively for improvement. Optical proximity correction (OPC) is widely used to get the desired features. Modified illuminations, such as off-axis illumination (OAI), are implemented to improve quality of certain features.

With more RET involved, the manufacturing cost, especially the mask cost, increases dramatically. Mask writers use e-beam to make the features, expensing more than 40% of total mask cost [1]. OPC increases the complexity of mask and data preparation/computation time by eight times in a 90nm design, comparing to a 0.35μm technology [2]. Inspection time also increases 4X. To lower the mask cost, it is necessary for layout synthesis tools to understand the lithography effects. A maze routing algorithm is proposed in [3] to reduce the OPC cost. In [4], a post-routing optimization algorithm is proposed to reduce the edge placement error (EPE). All these techniques are based on the traditional on-axis illumination.

Off-axis illumination (OAI) is introduced recently to improve the printability of dense features. It allows high order frequency information of patterns pass through the illumination system. However, OAI also brings up the "forbidden pitch" problem [5]. Although it provides significant process enhancement, design complexity, such as the number of design rules, will quickly explode.



(a) Without dummy metals inserted



(b) Dummy Metals are inserted to achieve uniformity

Fig. 1. Simulation results from Calibre. Without dummy metals inserted , the wires cannot be printed correctly even after OPC in (a). With dummy metals inserted, there are very little errors in (b). Defocus is considered in the aerial image simulation.

One solution is to improve the layout uniformity. It can maximize the yield and reduce design overhead. Restricted design rules (RDR) are proposed to use single pitch in layout [6]. Scattering bar is used to imitate the uniform environment for the lithographic system [7]. It can enhance the process window for poly gate. The extreme case is the regular fabric to maximize the yield and minimize design impact [8]. Regular contact design for standard cell is also proposed in [9] to improve the yield. The regularity is strongly preferred beyond the 90nm technology node due to the non-uniform and nonlinear properties of lithography equipment [10].

Assist features can be used to introduce the uniformity

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needed for photolithography. Sub-resolution assist features (SRAF) are widely used to improve the printability of poly gates. In the metal layers, dummy metal wire segments can be the same width as the primary features. Figure 1 shows that the layout becomes more uniform with the dummy metals inserted. Calibre [11] simulation results show printability is substantially improved. Without dummy metals, primary metal wires cannot be printed correctly even with OPC.

However, process variations make the performance harder to predict, and bring low yield issue. Excessive coupling capacitance from printable dummy metals may bring more severe manufacturing problems. SRAF dummy metals, in form of a set of non-printable parallel thin wires, can reduce the coupling capacitance. However, the optimal SRAF insertion is hard to find and involves model-based simulation [12]. Larger number of SRAF are needed for uniformity, which bring more complicate features on the mask. The cost will increase due to both the longer mask preparing and writing time. Moreover, this type of uniform environment cannot achieve the same depth of focus as printable dummies. We define the *lithography cost* as the total cost from mask and RET/process expense. The trade-off between excessive coupling and lithography cost from dummy metals must be considered while achieving the uniformity in the layout design.

In this paper, we propose a novel dummy metal insertion method to achieve the uniformity for the photolithography. An optimal algorithm is proposed to determine the dummy metal insertion efficiently, considering both coupling and lithography cost. Our main contributions in this paper include:

1. This is the first work to use both printable and non-printable assist feature for metal layers to improve the yield.

2. The trade-off between lithography cost and coupling capacitance are considered. A closed form equation is derived to guide the dummy insertion procedure.

3. An optimal algorithm is proposed to solve the coupling-aware dummy insertion problem.

The rest of this paper is organized as follows. In Section 2, we discuss the lithography cost and coupling capacitance issues related to dummy metals, and formulate the dummy metal insertion problem. In Section 3, optimal dummy metal insertion for a region is discussed. An algorithm is proposed in Section 4, and its optimality is proved. We show some experimental results in Section 5 and conclude the paper in Section 6.

II. Layout Uniformity, Lithography and Couping Capacitance

With continuous interconnection scaling down, RET used in poly layer, such as OAI, OPC and assist features, are now implemented in metal layers [13]. The OAI technology is introduced in 90nm technology and will be extensively used in future technology nodes [14].

Sub-resolution assist features (SRAF) are widely used in poly layer to solve the forbidden pitch problem brought by OAI. The size of SRAF is large enough to get desired improvement, but also small enough not to form exposed pattern on the wafer. However, in a region without diffusion area underneath, it is possible to use assist features with the same width as the primary feature. This kind of assist feature will leave as a real feature on the wafer, we call it printable assist feature (PAF). As an assist feature without printability requirement, PAF needs no OPC corrections.

Both PAF and SRAF can improve the uniformity of layout. However, SRAF brings a higher lithography cost. Optimal insertion of SRAF usually needs model-based method, which leads to a longer mask preparation time. More SRAF dummies than PAF dummies are needed to achieve similar Depth of Focus (DOF), bringing more features when writing a mask. E-beam is currently used to write the features on the mask. It will use small rectangles to print desired features. The writing time is approximately proportional to the perimeter of all features. Assume we need q parallel thin metal SRAF to act as one PAF dummy metal, the perimeter of dummy features will increase about $(q-1)$ times. Using SRAF as the dummy metals will increase lithography cost dramatically when q increases.

Another issue brought by SRAF is that the DOF cannot achieve the same level as that of PAF, as shown in Figure 2. With fewer SRAF in parallel to replace the PAF, the EPE increases faster for larger defocus. We define lithography cost M as

$$M = l(a(q-1) + b\Delta\text{DOF}) \tag{1}$$

to estimate the additional lithography cost brought by SRAF, where a and b are constants, and l is the total length of inserted SRAF. ΔDOF is the decrease of depth of focus if SRAF is used inserted instead of PAF. Both terms in M will increase when more SRAF dummies are inserted. Ignoring the small DOF change with a relatively large q, we will use $M = l(q-1)$ as the simplified cost function in the rest of this paper.

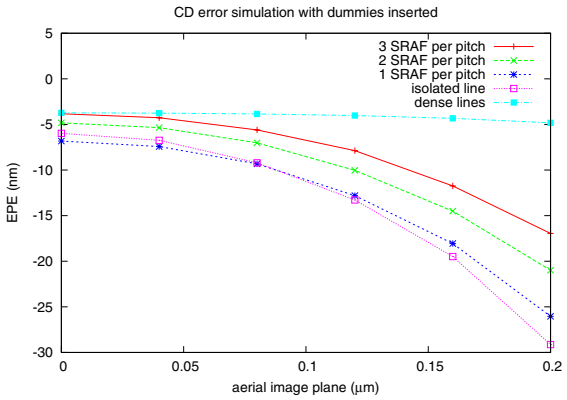


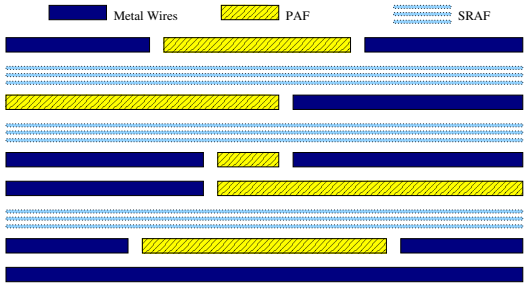
Fig. 2. Simulation results of DOF. The dense lines have the smallest EPE across all defocus levels and hence the best DOF. A larger EPE indicates a larger critical dimension (CD) error.

PAF will make features more uniform and thus improve printability better. However, PAF will leave printed metals on the wafer, which will increase the coupling capacitance. Adding PAF everywhere will increase the coupling capacitance dramatically. The coupling capacitances introduced by PAF

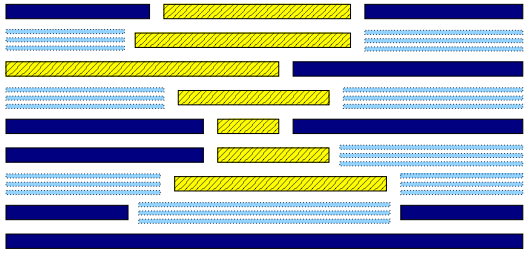
dummies can be evaluated by the closed-form equation in [15] as shown in Equation 2

$$C_X = l\frac{C_0}{S^\alpha}, \tag{2}$$

where l is the length of PAF, and S the spacing between main feature and PAF. C_0 and α are technology related constants, $\alpha \in (1, 2)$ for the current technology. The circuit performance will degrade by additional coupling capacitance. Although a circuit has passed the timing analysis before making the mask, these excessive coupling capacitance, which is not considered before tape-out, could lead to lower yield.



(a) One insertion solution



(b) A better dummy insertion solution

Fig. 3. Examples for coupling-aware SRAF/PAF dummy insertion. Solution in (b) is preferred with smaller coupling and lower lithography cost than the one in (a).

Consider the trade-off between the coupling and the lithography cost introduced by dummies, we want to minimize the lithography cost M, *i.e.* using minimum number of SRAF dummies, while reducing couping effectively for yield improvement. An intelligent way to decide the PAF/SRAF insertion is needed. An example is shown in Figure 3. Inserting PAF everywhere can surely achieve the best uniformity and thus best printability. To reduce the coupling capacitance, one solution is shown in Figure 3(a) with some PAF replaced by SRAF (q=3 here). 30% coupling capacitance is reduced. However, with carefully design, a better solution is shown in Figure 3(b), the lithography cost M decreases 5% while the coupling capacitance is also reduced to 76.7%, compared to the case in Figure 3(a).

We formulate a coupling-aware dummy metal insertion problem shown as below.

Coupling-aware Dummy Metal Insertion (CDMI) Problem. *Given a layout with metal wires routed, find a dummy metal insertion solution that minimize the lithography cost M. With the smallest possible number of SRAF dummies, keep the coupling capacitance no more than C_X*

III. Dummy Metal for a Free Region

To find an optimal solution for CDMI problem, we first partition the layout into a set of free regions. These regions are free space for dummy metal insertion. It can have one metal wire on its top and the other on its bottom. No other metals exist in free region as shown in Figure 4. There will be no interaction between the dummy metals that belong to different free regions. For a region with metal on only one boundary, we can treat it as a half region which will be discussed later.

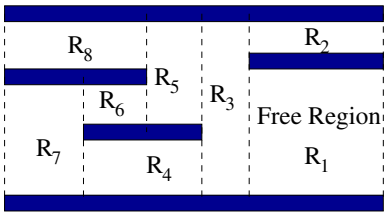


Fig. 4. Layout is partitioned into free regions. Dummy metals can be inserted for different free regions independently.

Dummy metals will be inserted into free regions to make uniform structures for photolithography. So the insertion locations are uniformly distributed and fixed, which are defined as tracks. All tracks have the same length L as the length of the region. Both SRAF and PAF dummy metals can be inserted as shown in Figure 5. For a region with k tracks, dummy metals have a total length kL. Assume the total length of PAF is x, the SRAF has total length $kL - x$.

To find a optimal insertion for the free region, we should maximize x with a certain coupling capacitance constraint. Equivalently, if we fix x and find an insertion solution with minimized coupling capacitance, it's also an optimal solution. We have several observations for this problem.

First, it can be shown that the PAF in different tracks should be aligned as shown in Figure 5. This will maximize their overlap and reduce the coupling capacitance introduced. The metals are not necessarily aligned on the boundary. The position of PAF in a track is not related to the coupling capacitance as long as the overlap is maximized. To simply the analysis, we assume the PAF are aligned on the right.

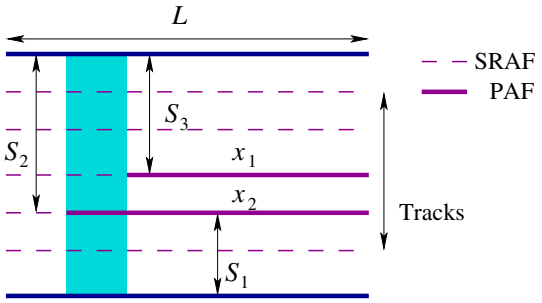


Fig. 5. Dummy metals are inserted for uniformity in a free region. Solid lines are PAF, and dashed lines are SRAF. One dashed line corresponds to a set of SRAF dummy metals, which are thin parallel wires. This region has 5 tracks. Its length is L.

Secondly, the PAF closer to the middle of the free region

should be the longest. As shown in Figure 5, assuming x_1 is closer to the middle track, we have $S_2 > S_3 > S_1$ and $x_1 < x_2$. The coupling capacitance in the shaded region is

$$\frac{C}{C_0} = \frac{x_2 - x_1}{S_1^\alpha} + \frac{x_2 - x_1}{S_2^\alpha}. \tag{3}$$

If we change x_1 and x_2 to be the same length as $(x_1 + x_2)/2$, the capacitance in the shaded area is

$$\begin{aligned} \frac{C'}{C_0} &= \frac{x_2 - x_1}{2S_1^\alpha} + \frac{x_2 - x_1}{2S_3^\alpha} + \frac{x_2 - x_1}{2S_0^\alpha} \\ &\leq \frac{x_2 - x_1}{2S_0^\alpha} + \frac{x_2 - x_1}{S_1^\alpha} \\ &< \frac{x_2 - x_1}{S_2^\alpha} + \frac{x_2 - x_1}{S_1^\alpha} = \frac{C}{C_0}, \end{aligned} \tag{4}$$

where S_0 is the distance between top and bottom metal wires. This inequality shows a longer wire in the middle is always preferred. If the region has even number of tracks, PAF dummy metals at middle two tracks should have the same longest length among all dummy metals. This also can be proved by Equation 4.

The dummy metal at the middle can act as shield to couplings. It prevents the coupling from PAF on top of it to the bottom metal of the free region, and vice versa. When we study the optimal insertion for the region, we can divide the free region into two symmetric parts, find the optimal solution for the half region and duplicate it to the other half. The final insertion solution will be optimal for the whole region.

Consider one half of the free region in Figure 6, the total number of tracks of the free region can be $k = 2m$ or $k = 2m-1$. Assuming the pitch is P and wire width is $W = (1-\beta)P$, where $\beta < 1$. $S_i = (i+\beta)P = b_i P$. The distance between top and bottom wires of free region is $S_0 = b_0 P = (k+\beta)P$. As discussed previously, the length of PAF is monotonically non-decreasing, $x_1 \leq x_2 \cdots \leq x_m$. Assuming $x = \sum_{i=1}^{m} x_i$, The coupling capacitance introduced by dummy metals is

$$\begin{aligned} \frac{C}{C_0} &= \sum_{i=2}^{m} \frac{x_i - x_{i-1}}{S_i^\alpha} + \frac{x_1}{S_1^\alpha} - \frac{L}{S_0^\alpha} \\ &= \frac{x}{P^\alpha b_m^\alpha} - \frac{L}{P^\alpha b_0^\alpha} \\ &\quad + \sum_{i=1}^{m-1} \frac{x_i}{P^\alpha} \left(\frac{1}{b_i^\alpha} - \frac{1}{b_{i+1}^\alpha} - \frac{1}{b_m^\alpha} - \frac{1}{b_0^\alpha} \right) \end{aligned} \tag{5}$$

Let p be the smallest integer that satisfies

$$\frac{1}{b_p^\alpha} - \frac{1}{b_{p+1}^\alpha} < \frac{1}{b_m^\alpha} + \frac{1}{b_0^\alpha}. \tag{6}$$

p increases slowly with m as shown in Figure 7. It can be approximated as

$$p \approx \left(\frac{\alpha}{(m+\beta)^{-\alpha} + (k+\beta)^{-\alpha}} \right)^{\frac{1}{\alpha+1}} - \beta + 0.5. \tag{7}$$

Since α is close to 1 and bounded in $(1, 2)$, p is decided by $m^{1/2}$ to $m^{2/3}$, which increases slowly with m. For the free region, there will be $t = k - 2p + 2 \geq k/2$ tracks inserted with PAF dummy metals. If we insert PAF with a total length x to the free region, the total coupling capacitance introduced by dummy metals is

$$\frac{C}{C_0} = x \left(\frac{2}{(k-2p+2)S_p^\alpha} + \frac{2}{S_0^\alpha} \right) - \frac{2L}{S_0^\alpha}. \tag{8}$$

Here we assume $x \leq tL$. If $x > tL$, we have to insert more PAF to other tracks after we fully insert PAF to those t tracks. However, two new free regions are formed with t tracks fully inserted. We can again find optimal insertion for those new free regions. Notice these free regions only have one routed wire on its boundary. The optimal insertion is the same to insert PAF to half of the free region from Equation 5. If we insert PAF with a total length x to a new free region, the total coupling capacitance introduced by dummy metals is

$$\frac{C}{C_0} = x \left(\frac{1}{(k-p+1)S_p^\alpha} + \frac{1}{S_0^\alpha} \right) - \frac{L}{S_0^\alpha}. \tag{9}$$

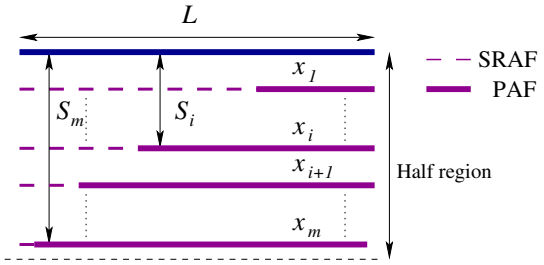


Fig. 6. Top half of free region with m tracks. It is symmetric to the bottom half.

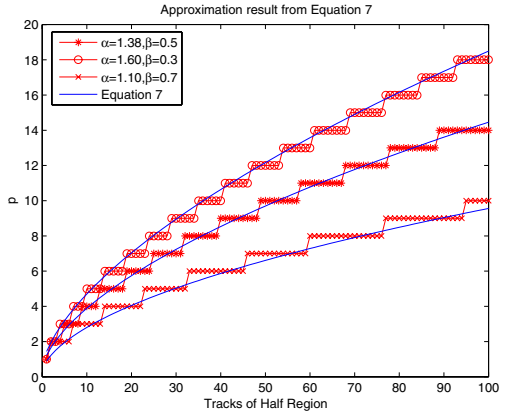


Fig. 7. p slowly increases with m. Equation 7 is a good approximation to the minimum p that satisfies Equation 6.

IV. Optimal Dummy Metal Insertion Algorithm

To solve the CDMI problem, we introduce the capacitance to lithography cost (CLC) ratio. We want to minimize the lithography cost subject to a bound on coupling capacitance. So it is preferred to introduce more PAF dummy metals with

less coupling capacitance overhead. As discussed previously, the coupling capacitance C is a function of the total length x of PAF inserted. If the total length of PAF is x_0, the CLC ratio is

$$CLC = \frac{\partial C}{\partial x}\Big|_{x=x_0}. \tag{10}$$

x_0 corresponds to a certain lithography cost M as discussed in Section 2. So CLC means how much coupling capacitance is introduced at a certain lithography cost. Inserting PAF in tracks with lower CLC is always preferred. Because it brings less coupling capacitance with the same lithography cost.

Theorem 1 *The CLC ratio only related to the total number of tracks in a free region, and the boundary condition of the region.*

Proof: We take derivative on Equation 8 and 9 and get

$$\text{CLC} = \begin{cases} C_0 \left(\dfrac{2}{(k-2p+2)S_p^\alpha} + \dfrac{2}{S_0^\alpha} \right) & \text{case I} \\ C_0 \left(\dfrac{1}{(k-p+1)S_p^\alpha} + \dfrac{1}{S_0^\alpha} \right) & \text{case II} \end{cases} \tag{11}$$

Case I has two metal wires on the boundaries of the free region. Case II only has one. Since p is also a function of k as shown in Equation 6, Equation 11 is only a function of the total track number k. □

With Theorem 1, we can group the free regions with the same CLC ratio and insert dummy metals for them simultaneously. Since we want to minimize the lithography cost, the algorithm will start with the regions with the smallest CLC ratio. After insertion, new free regions could be formed if there is still coupling capacitance budget left. Then, our algorithm will iteratively insert dummy metals as many as possible to those regions with the smallest CLC ratio until it reaches the coupling capacitance constraint. SRAF dummy metal will be inserted to achieve uniformity hereafter. The following theorem is needed for the correctness of our algorithm.

Theorem 2 *Before the coupling capacitance constraint is reached, the PAF dummy metals can be inserted to t tracks in a free region with identical length L. It forms two new free region with larger CLC ratios.*

Proof: It can be shown that as many as dummy metals should be added if the constraint allows as discussed in Section 4. So the PAF dummy metals will fully use the tracks. Thus, only two free regions will be formed after insertion. For the new free regions, the new k',S'^{α}_{p} and S'^{α}_{0} are smaller than the original one. It can be shown that $k' \leq k/2$, $S'^{\alpha}_{p} \leq S^{\alpha}_{p}/2$ and $S'^{\alpha}_{0} < S^{\alpha}_{0}/2$. Moreover, p increases slowly with k, the new CLC from Equation 11 will be larger. So dummy metals should be inserted in the original free region first , and then the new free regions. □

Theorem 2 shows we can iteratively solve the CDMI problem. Assuming we can group the free regions into

$$G = \{g_1, \ldots, g_i, \ldots\},$$

Algorithm 1: CDMI Algorithm

Input: Layout with metal lines
Total coupling capacitance constraint: C_X
Output: Layout with dummy metals inserted

```
begin
    Partition the layout into free regions;
    Create groups of regions G;
    C = C_X;
    while C > 0 do
        find g_i ∈ G with minimum CLC;
        p = FINDP(k_i);
        C_i = L_i * CLC(g_i);
        if (C ≥ C_i) then
            Insert PAF to all t tracks in g_i;
            new free regions g'_i formed;
            G = G ∪ g'_i;
            C = C − C_i;
        else
            L' = C/CLC(g_i);
            C = 0;
            for each free region in g_i do
                l is the length of this free region;
                L_c = L' * l/L_i;
                Insert PAF with length L_c for t tracks;
            end
        end
    end
    Insert SRAF to all left tracks;
end
```

Each g_i has a group of free regions with a CLC ratio CLC(g_i). And we also use L_i to annotate the total length of the free regions in g_i. And the regions in g_i has the same number of tracks k_i. With these notations, Algorithm 1 is proposed to solve CDMI problem exactly.

In Algorithm 1, FINDP(k) is a function to calculate p according to Equation 6. If the constraint allows, we insert PAF to all t tracks in g_i by Theorem 2. If there is not enough coupling budget, we just insert PAF dummy metals to part of the tracks as previously discussed.

Theorem 3 *Algorithm 1 will insert dummy metals with a minimum lithography cost. It guarantees to satisfy the coupling capacitance constraint.*

Proof: In Algorithm 1, the PAF is always inserted with a minimum CLC ratio. After inserting PAF, new free regions are updated. However, all regions remained must have a higher CLC according to Theorem 2. So every PAF insertion is optimal for the existing free regions. In the last step, although less PAF are inserted due to the coupling capacitance constraint, the optimum still holds. So every iteration in Algorithm 1 will give an optimal insertion to the CDMI problem with a smaller coupling constraint, and reduce it to a smaller problem with less regions and updated coupling constraint. When Algorithm 1 finishes, it will reach the optimum for the original problem. Each iteration, we always maximize the usage of PAF dummy metals.

Eventually, we use as many PAF as possible. The lithography cost is minimized. □

After partition the layout into free regions, Algorithm 1 finishes very quickly since p can be the same for different k. The size of G will decrease very fast during the iteration. If we assume there are totally N free regions, the complexity of our algorithm is $O(N)$.

V. Experimental Results

We applied our algorithm to a set of layouts. The dummy metals are inserted with a coupling capacitance constraint. Simulations are performed by Calibre tools [11] to confirm the printing quality. The optical parameters settings are: NA=0.75, $\lambda = 193$nm. The off-axis light source is at $(0.5, 0)$ with a partial coherent coefficient $\sigma = 0.3$. The fragmentation of OPC is set to high with a 10nm grid. The metal wires are 80nm wide with a 180nm pitch. Capacitance is obtained by Equation 2 with $\alpha = 1.38$. Figure 8 shows a part of the dummy metal insertion results by Algorithm 1. Notice because of the coupling capacitance will reduce almost quadratically along the distance. The dummy metal are inserted in most spaces, which leads to a dense and uniform metal layer. It can also help CMP procedures.

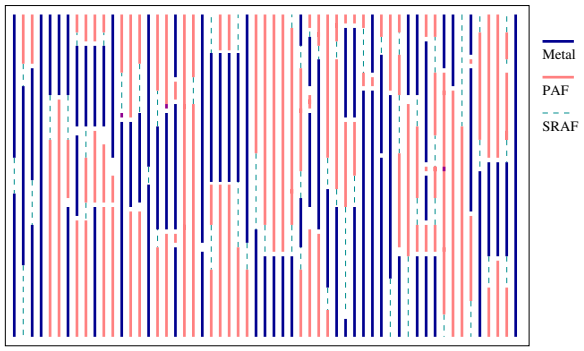


Fig. 8. Results from the dummy metal insertion algorithm. Dark lines are routed metal wires. Light lines are PAF. Doted lines are SRAF.

Table I shows the comparison of results from the examples in Figure 8. Alought *Method I* has less lithography cost, it doesn't meet the couping constraint. We can insert PAF dummy metals everywhere as *Method I*, which leads to excessive coupling. Or we can use SRAF for all dummies as *Method II*, which increases the lithography cost. Our algorithm can find the optimal solution, considering the coupling and lithography cost trade-off.

TABLE I
Results comparison

	Method I	*Method II*	*Our method*
M	0.81X	2.4X	1X
C_X	1.12X	0.64X	1X

VI. Conclusion

With new RET intensively used in sub-100nm technologies, uniform layout structure is preferred to maximize the yield with a reasonable lithography cost. We proposed a dummy metal insertion methodology to maintain the uniformity with coupling capacitance consideration. An optimal algorithm is proposed to determine the dummy metal insertion. This post-routing techniques can potentially improve the printability with a lower lithography cost and controlled coupling capacitance.

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