# Low-Power High-Speed 180-nm CMOS Clock Drivers

**Tadayoshi Enomoto, Suguru Nagayama, and Nobuaki Kobayashi**

**Chuo University, 1-13-27 Kasuga, Bunkyo-ku, Tokyo 112-8551, Japan**
**tenmt@ise.chuo-u.ac.jp**

**Abstract - The power dissipation ($P_T$) and delay time ($t_{dT}$) of a CMOS clock driver were minimized. Eight test circuits, each of which has 2 two-stage clock drivers, and a register array were fabricated using 0.18-µm CMOS technology. The first and second stages of the driver consisted of a single inverter and *m* inverters, respectively, and the register array stage was constructed with *N* delay flip-flops (D-FFs). A single inverter in the second stage drove *N*/*m* D-FFs where *N* was fixed at 40 and *m* varied from 1 to 40. Minimum $P_T$ and $t_{dT}$ were 251 µW and 0.640 ns, respectively and were both obtained at an *m* of 8. These values were 48.6% and 29.4% of maximum $P_T$ and $t_{dT}$, respectively. Simulated and measured results agreed well with these SPICE simulated results.**

## I. Introduction

The power dissipation ($P_T$) of clock drivers is extremely large, 30 to 50% of the total power dissipation of a CMOS LSI chip, such as video codec LSIs, multi-media processors, etc [1]. Therefore, to significantly reduce the total power dissipation of CMOS LSI chips, the power dissipation of clock drivers must be minimized. The power dissipation ($P_T$) of CMOS random logic circuits is the sum of the power dissipation ($P_D$) due to the dynamic current, and power dissipation ($P_S$) due to the short-circuit current [2]. For conventional random logic circuits, $P_S$ is much smaller than $P_D$, which means $P_T$ is approximately equal to $P_D$. However, the $P_S$ of a clock driver that consists of multi-stage inverter trees, each of which has a large number of delay flip-flops (D-FFs), is considerably larger. Furthermore, the large number of D-FFs also lengthens the signal propagation delay times ($t_{dT}$). Thus, clock drivers must be designed in such a way that both $P_T$ and $t_{dT}$ are minimized.

## II. Circuit Design and Fabrication

An MPEG4 8-bit absolute difference accumulation (ADA) circuit for motion estimation consists of an 8-bit absolute difference circuit, a 16-bit ripple carry type accumulator, and registers with 40 D-FFs each [3]. The test circuit shown in Fig. 1(a) was designed for this type of ADA circuit using 0.18-µm double-well, 5-layer interconnection CMOS technology. It consists of 2 two-stage clock drivers and a register array. These clock drivers generate a pair of complement clock pulses (*cl* and *clb*). The register array is constructed with 40 D-FFs. A circuit diagram of this type of D-FF is also shown in Fig. 1(b). There are one and *m* inverters in the first and second stages in the clock drivers, respectively. The number of fan-outs of the inverter in the first stage is *m*, and the number of D-FFs that are driven by a single inverter in the second stage is *n* (=*N*/*m*, where *N* is the

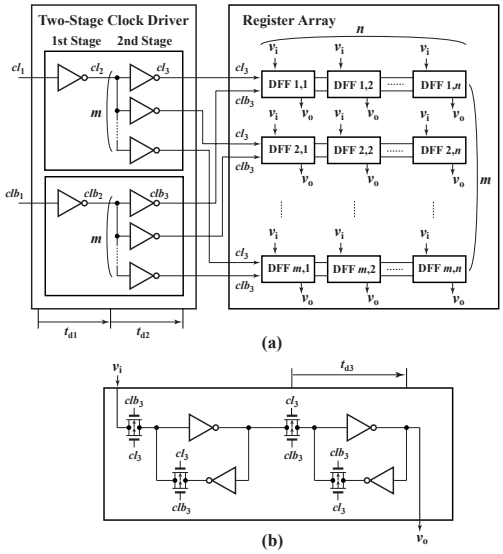


Fig. 1. A circuit diagram of a CMOS test circuit. (a) Clock drivers and a register array. (b) D-FF.

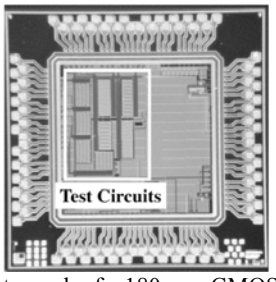


Fig. 2 Photograph of a 180-nm, CMOS LSI chip with 8 test circuits.

number of D-FFs). The *m*×*n* (=*N*=40) of the eight test circuits are 1×40, 2×20, 4×10, 5×8, 8×5, 10×4, 20×2, and 40×1.

A CMOS LSI chip in which the eight above test circuits are included is shown in Fig. 2. The chip was fabricated using 0.18-µm CMOS technology. The areas of the test circuits and the LSI chip were 1,025×744 µm$^2$ and 2.8×2.8 mm$^2$, respectively. Both the nMOSFET and pMOSFET have gate lengths of 0.18 µm. The channel widths of the nMOSFET and pMOSFET are 2.05 and 6.15 µm, respectively, and their threshold voltages are 0.435 V and -0.415 V, respectively.

## III. Circuit Characteristics

### 3.1 Speed Performance

The SPICE simulated output waveforms at various nodes in the test circuit with *m*=1 and *n*=40 are shown in Fig. 3(a).

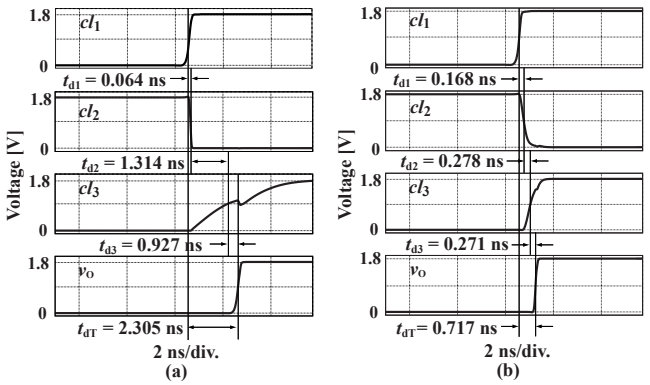


Fig. 3. Simulated output waveforms at various nodes in test circuit with $N$ = 40. (a) $m$ = 1 and $n$ = 40. (b) $m$ = 8 and $n$ = 5.

$cl_1$, $cl_2$, and $cl_3$ are inputs of the first stage, second stage, and register array, respectively, and $v_o$ is the output of D-FF. The simulated delay times of the first ($t_{d1}$), second ($t_{d2}$), and third stages ($t_{d3}$) (i.e., $t_{d3}$ is the set-up time of D-FF), are 0.064, 1.314, and 0.927 ns, respectively, and the total delay time ($t_{dT}$=$t_{d1}$+$t_{d2}$+$t_{d3}$) is 2.306 ns. The rise time ($t_r$) and fall time ($t_f$) (not shown) of $cl_3$ are extremely long because a single inverter in the second stage must drive a large number of D-FFs (i.e., $n$=40). $cl_1$, $cl_2$, $cl_3$, and $v_o$ of the test circuit with $m$ = 8 and $n$ (=$N$/$m$) = 5 are also shown in Fig. 3(b). $t_{d1}$, $t_{d2}$, and $t_{d3}$ are 0.168, 0.278, and 0.271 ns, respectively. $t_{d2}$, and $t_r$ and $t_f$ (not shown) of $cl_3$ are considerably reduced because the number of load D-FFs is optimized to 5.

The solid lines in Fig. 4 represent the average $t_{dT}$, $t_{d1}$, $t_{d2}$, and $t_{d3}$ for $N$ = 40 as a function of $m$. $t_{d1}$ increases linearly, while $t_{d2}$ is inversely proportional to $m$ (i.e., $t_{d2}$ is proportional to $n$=$N$/$m$). $t_{d3}$ is also inversely proportional to $m$ because $t_r$ and $t_f$ of $cl_3$ decrease as $m$ increases. Thus, as $m$ increases, $t_{dT}$ quickly decreases, reaches a minimum at about $m$=8, and then slowly increases. The minimum $t_{dT}$ (0.717 ns), at $m$=8, is considerably reduced, to 31.1% of the $t_{dT}$ (2.305 ns) with $m$=1 (Fig. 3). Similar $t_{dT}$ performances were obtained for various $N$, from 20 to 320.

### 3.2 Power Dissipation

Figure 5 shows the experimentally measured and simulated power dissipations of the first stage ($P_1$), second stage ($P_2$), register array stage ($P_3$), and all stages ($P_T$=$P_1$+$P_2$+$P_3$) in the test circuits. The measured results of the fabricated test circuits (Fig. 2) correlate well with the simulated results. $P_1$ and $P_2$ increase, while $P_3$ decreases, as $m$ increases. $P_2$ consists of dynamic power consumed by MOSFET switches in the 40 D-FFs and short-circuit power consumed by $m$ inverters in the second stage. The former is almost constant (about 110 μW) and independent of $m$, but the later is proportional to $m$. $P_3$ decreases quickly as $m$ increases in the region where $m$ is less than 8, while it decreases slowly in the region where $m$ is greater than 8, since $t_r$ and $t_f$ of $cl_3$ supplied to the register array stage are reduced by increasing $m$. That is, short-circuit currents in

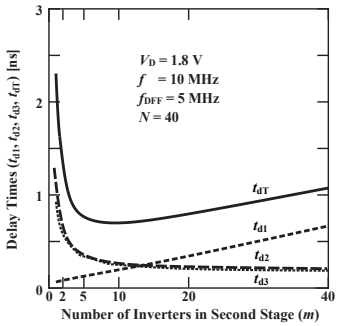


Fig. 4. Simulated delay time ($t$) of test circuits.

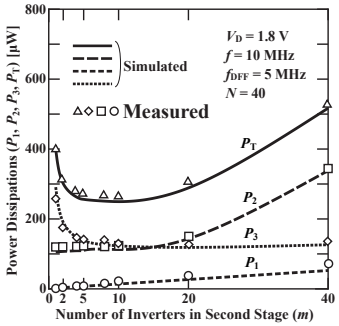


Fig. 5. Measured and simulated power dissipation of test circuits.

the D-FFs decrease with an increase in $m$. $P_3$ with $m$ = 8 is 126 μW that is 43.3% of the $P_3$ (291 μW) with $m$ = 1. Thus, $P_T$ quickly decreases, reaches a minimum at $m$ = 8, and then slowly increases as $m$ increases. The minimum $P_T$ (251 μW) of the test circuit with $m$ = 8 is greatly reduced to 48.6% of the $P_T$ with $m$ = 40 (517 μW). Similar $P_T$ characteristics were also obtained for various $N$ (20 to 320).

## IV. Conclusion

A 0.18-μm CMOS test circuit consisting of a two-stage clock driver (with one and $m$ inverters in the first and second stages , respectively) and a register array with 40 delay flip-flops (D-FFs), was fabricated. The power dissipation and delay time of an optimized test circuit were successfully reduced to 1/2 and 1/3 of the maximum power dissipation and delay time, respectively.

## References

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