A 0.35um CMOS 1,632-gate-count Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI

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***Abstract*— A Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI (ZO-DORGA-VLSI) has been developed. It is based on a concept using junction capacitance of photodiodes and load capacitance of gates constructing a gate array as configuration memory and removing static memory function to store a context. In this paper, the performance of a 1,632 ZO-DORGA-VLSI, which was fabricated using a 0.35 μm – 4.9 mm square CMOS process chip, is presented. In addition, the design of an over 10,000 ZO-DORGA-VLSI is presented.**

I. Introduction

In recent years, optically programmable gate arrays (OPGAs) [1][2][3] have been proposed, in which an optical holographic memory is introduced and connected directly to the gate array part of a VLSI circuit. These devices can provide rapid reconfiguration and numerous reconfiguration contexts. Currently, OPGAs have achieved performance that offers a hundred reconfiguration contexts and a 16-20 μs reconfiguration period. However, the OPGAs present a drawback: the VLSI part's gate density is very low. A previously fabricated OPGA-VLSI had only 80 gates because of serial transfer architecture and static memory function to store a context. Furthermore, it is difficult to improve the 16-20 μs reconfiguration speed to support clock-by-clock reconfiguration. Moreover, the gate array can not be used during reconfiguration.

To improve those two weak points of OPGAs, a Zero-Overhead Dynamic Optically Reconfigurable Gate Array (ZO-DORGA) was developed [4], [5]. In these devices, the gate array can be reconfigured in nanoseconds and be used during reconfiguration. The reconfiguration overhead has been decreased using the load capacitance of gates used to construct a gate array as a configuration memory. The ZO-DORGA presents two advantages: the ZO-DORGA can achieve a large gate count and its reconfiguration speed can reach nanoseconds without any overhead. In this paper, the performance of a 1,632 ZO-DORGA-VLSI that was fabricated using a 0.35 μm - 4.9 mm square CMOS process chip, is presented. Furthermore, a design of an over 10,000 ZO-DORGA-VLSI is presented.

II. Zero-overhead dynamic optical reconfiguration circuit

A single-bit optical reconfiguration circuit in conventional OPGAs comprises: photodiodes; static memory functions of a latch and a bit of memory; and a part of a serial transfer. However, the static memory function requires a large implementation area, which strictly prohibits the realization of high gate-count ORGAs. Furthermore, OPGAs require 16 μs - 20 μs overhead for each reconfiguration procedure. That reconfiguration overhead is too great: the reconfiguration operation consumes 99% of the entire operation time when the gate array is reconfigured at every 10 ns operation. Therefore, to improve those two issues, a ZO-DORGA has been developed. The optical reconfiguration circuits of the ZO-DORGA are based on a concept using junction capacitance of photodiodes and load capacitance of gates used for constructing a gate array as configuration memory. The state of the gate array is maintained during reconfiguration using load capacitance of the gates that constitute the gate array. Consequently, the zero-overhead dynamic optical reconfiguration circuit allows parallel execution of the reconfiguration operation and the circuit operation implemented on the gate array. The Schematic diagram of the zero-overhead dynamic optical reconfiguration circuit is shown in Fig. 1. A pass transistor functions block off the connection between the gate array and dynamic optical reconfiguration circuit during reconfiguration. Each load of inverter gates, transmission gates, and so on composing the gate array is used to maintain the gate array state during the gate-array reconfiguration.

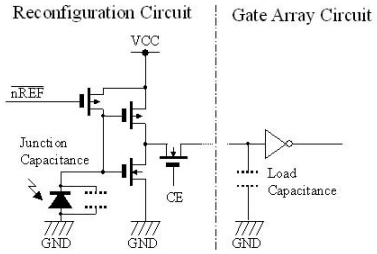

Fig. 1. Schematic diagram of a zero-overhead dynamic optical reconfiguration circuit.

III. 1,632-gate-count DORGA-VLSI

A new 1,632-gate-count DORGA-VLSI chip was fabricated using a 0.35 μm – 4.9 mm square CMOS process chip. Figure 2 shows the CAD layout and photograph. The acceptance

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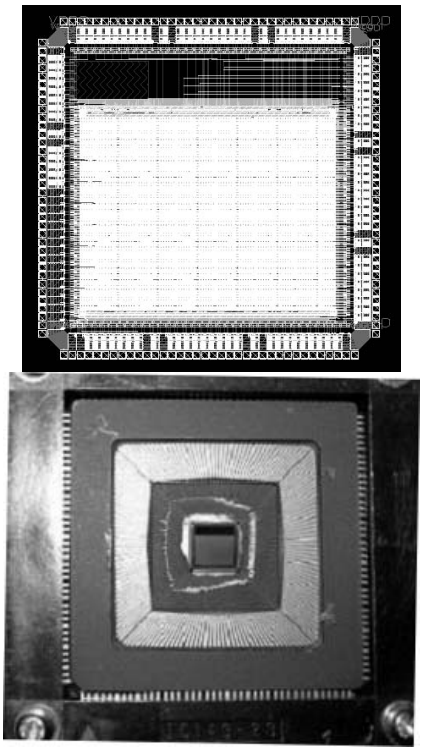

Fig. 2. CAD layout and chip photograph of a fabricated DORGA chip using a 0.35 μm – 4.9 mm square CMOS process chip.

size of photodiodes is 9.5 $\mu m \times$ 8.8 μm. The photodiodes were constructed between N+ diffusion and the P-substrate. Photodiode cells are arranged at 34.5 μm horizontal intervals and at 33.0 μm vertical intervals. This design incorporates 6,213 photodiodes. In this design, considering the resolution of optical components and simplified justification of the positioning between a VLSI part and an optical part, photodiodes and their spacing were designed to be large. The top metal layer was used for guarding transistors from light irradiation; the other two layers were used for wiring. The gate array of the DORGA-VLSI is an island style array. In all, 48 optically reconfigurable logic blocks (ORLBs) including two 4-input – 1-output LUTs, 63 optically reconfigurable switching matrices (ORSMs), and 6 optically reconfigurable I/O bits (ORIOBs) including 4 I/O bits were implemented in the DORGA-VLSI.

The photodiode response time was measured as less than 10.0 ns. We have also confirmed that the minimum pulse width extracted from HSPICE simulation results is less than 1 ns. Therefore, if a DORGA-VLSI chip has a short pulse generator in its own chip, the reconfiguration cycle is estimated as less than 12 ns. The retention time was measured as longer than 100 μs.

IV. Over 10,000-gate-count DORGA-VLSI

Using a 0.35 μm – 9.8 mm square CMOS process chip and the same ORLB, ORSM and ORIOB designs, we can produce a VLSI with greater than 10,000 gate count, as shown in Fig. 3. In this design, 336 ORLBs, 375 ORSMs, and 8 ORIOBs were implemented.

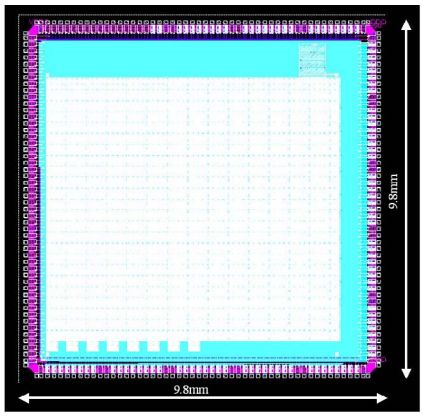

Fig. 3. CAD layout of a designed DORGA chip using a 0.35 μm – 9.8 mm square CMOS process chip.

V. Conclusion

In this paper, a 1,632 gate count ZO-DORGA-VLSI was presented. The ZO-DORGA architecture described herein achieved a high gate-count and rapid reconfiguration without any overhead. The reconfiguration cycle and retention time were confirmed as less than 12 ns and greater than 100 μs. Moreover, we have confirmed, using a 0.35 μm – 9.8 mm square CMOS process chip, that we can fabricate a VLSI with a greater than 10,000 gate count.

VI. Acknowledgment

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