A 10Gbps/channel On-Chip Signaling Circuit with an Impedance-Unmatched CML Driver in 90nm CMOS Technology

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Abstract— An on-chip signaling system consists of a CML driver, a differential transmission-line and a CML receiver is fabricated. We developed an impedance-unmatched driver for power reduction. The impedance-unmatched driver reduces the tail current of the CML buffer by tuning the load resistance. The designed circuit achieves 3mm, 10Gbps/channel on-chip signal transmission and the impedance-unmatched driver saves the energy per bit by 21% compared with a conventional impedance-matched driver.

I. Introduction

The on-chip interconnects are becoming a serious limitation of whole chip performance. To improve on-chip signaling, several methods have been discussed [1–4]. In on-chip signaling, the driver of on-chip long distance interconnects is the bottleneck of the bandwidth. Thus using CML buffers is a solution to improve on-chip signaling. CML (Current Mode Logic) buffer can operate in higher frequency and have tolerance to the common-mode noise compared with conventional CMOS inverters [5]. On the other hand, the power dissipation is larger because CML buffer require the static current flow.

We designed a 10Gbps signaling system using an impedance-unmatched CML driver. An impedance-unmatched driver can reduce the tail current by tuning the output resistance of the CML driver. We fabricated and measured the signaling system in a 90nm CMOS technology to demonstrate the proposed idea. The measurement results show that the designed circuit can transmit 10Gbps signal through 3mm on-chip differential transmission-line and the proposed design saves the energy per bit by 21% compared with the conventional impedance-matched driver.

II. Signaling system using an impedance-unmatched driver

We designed a 10Gbps signaling system on a 90nm technology. Figure 1 shows the structure of the targeted signaling system. The signaling system consists of a tapered CML driver, a differential transmission-line, a terminator and a CML receiver. As shown in Fig. 1, R_{D} is the output resistor and I_{tail} is a current source of CML. We assume the structure of the transmission-line as shown Figure 2. The differential characteristic impedance of the transmission-line is 75Ω and the attenuation of 3mm transmission-line is 3dB. The terminator at the receiver input is tuned to the characteristic impedance of the transmission-line in order to eliminate the effect of the reflected wave. Therefore impedance mismatch at the driver output is not a serious problem.

The basic design flow is discussed in Ref. [5]. The tail current I_{tail} is determined from the output voltage swing and the output resistance R_{D} of the driver. From the tail current I_{tail}, the size of the NMOS transistor is tuned from the square law of NMOS drain current. Thus, in conventional design, the all parameters of CML driver are determined from the output resistance which equals to the characteristic impedance of the

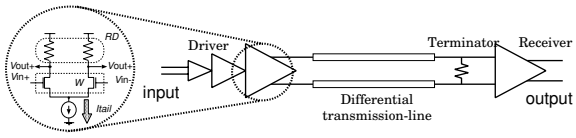

Fig. 1. Structure of the targeted signaling system.

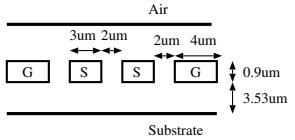

Fig. 2. Cross section of the differential transmission-line.

transmission-line. However in proposed design, we can tune the tail current I_{tail} and the gate width W by changing the output resistance R_{D}.

In order to evaluate the effect of impedance mismatching, we estimated the characteristics of CML drivers from pole frequency analysis. The pole frequency is determined from the resistance and the capacitance connected to the drain of the switching transistor. The pole frequency ω_{p} is expressed as

$$\omega_{\mathrm{p}} = \frac{1}{R_{\mathrm{D}}(C_{\mathrm{Tr}} + C_{\mathrm{parasitic}})}, \tag{1}$$

where C_{Tr} is the capacitance proportional to transistor size W and $C_{\mathrm{parasitic}}$ is the parasitic capacitances such as wire-to-wire capacitance. The transistor size is proportional to the tail current I_{tail} and inverse proportion to the output resistance R_{D}. If $C_{\mathrm{parasitic}}$ equals to 0, the pole frequency ω_{p} is constant against changing the output resistance R_{D}. However in real, the pole frequency degrades because of the parasitic capacitances $C_{\mathrm{parasitic}}$. Figure 3 shows the trade-off curve between the bandwidth and the power dissipation in circuit simulation. The solid line shows the pole frequency analysis of the driver. In the region where the output resistance is small, pole frequency degradation is small because the capacitance C_{Tr} is dominant and the total capacitance is almost proportional to the inverse of the output resistance R_{D}. Therefore in this condition, the impedance-unmatched driver can reduce the power dissipation with little degrading the pole frequency.

From Fig. 3, we determined the output resistance of the driver 75Ω due to meet the required specification to transmit the input signal at 10Gbps. Circuit simulations show that the input voltage swing that the CML receiver can sense the signal is 200mV. We set the output voltage swing of the driver to 340mV considering the attenuation and the noise margin. The driver circuit is a tapered buffer that the number of stages is 5 and the taper ratio is 1.73. Figure 4 shows the schematic of the designed circuit. The fabricated circuit includes an output buffer for measurement. The output buffer is tuned as the output impedance becomes 50Ω. In this work, the eye diagram is

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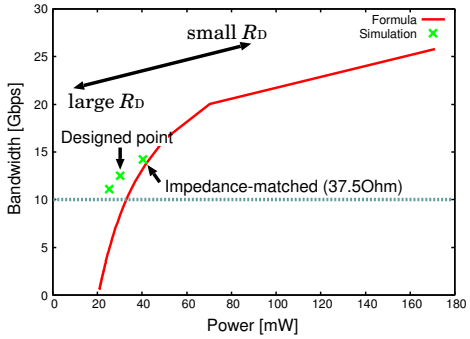

Fig. 3. Trade-off curve between the bandwidth and the power dissipation.

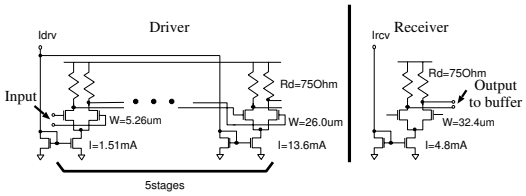

Fig. 4. Schematic of the designed circuit.

evaluated at the output of the output buffer. Figure 5 shows a micrograph of a fabricated chip.

III. Measurement Results

This section describes measurement results of the signaling system. We evaluated the eye-diagram at the output of the signaling system. The input pulse sequence is a 400mV peak-to-peak NRZ PRBS generated by a pulse pattern generator. The pattern length is $2^{23} - 1$. Table I shows the specification of the signaling system. Figure 6 shows the measurement result of eye-diagram at 10Gbps PRBS input and Fig. 7 shows the eye-diagram in circuit simulation. As shown Fig. 6, the eye-opening voltage was 86.2mV and was 7.2% larger as compared with simulation results. At 10Gbps transmission, the power dissipation and the energy per bit of the driver were 27.3mW and 2.18pJ/bit. If we use the conventional impedance-matched driver the power dissipation and the energy per bit of the driver are 40.3mW and 2.88pJ/bit. Therefore the proposed design saves the power dissipation by 32% and the energy per bit by 21%.

IV. Conclusion

This paper presented a design of on-chip signaling system. We show the measurement results of the signaling system of the low-power designed CML driver using impedance-unmatched driver. The signaling system using the proposed driver was fabricated on a 90nm technology. We verified the proposed driver can reduce the power dissipation by 32% and transmit PRBS input by measurement.

Acknowledgements

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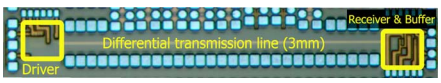

Fig. 5. Chip micrograph of the signaling system.

TABLE I
Specification of the proposed design and a conventional design.

	Proposal	Conventional †
Technology	90nm CMOS	
Supply Voltage	1.0V	
Transmission line	3mm	
Bandwidth	10Gbps/Channel	—
Max Bandwidth	12.5Gbps/Channel	14.0Gbps/Channel
Power(Driver)	27.3mW	40.3mW
Power(Receiver)	4.20mW	4.32mW
Energy/bit(Driver) ††	2.18pJ/bit	2.88pJ/bit
Energy/bit(Receiver) ††	0.336pJ/bit	0.309pJ/bit
Area(Driver) †††	$158\mu m \times 99.5\mu m$	—
Area(Receiver) †††	$42.8\mu m \times 28.1\mu m$	—

† The specification of a conventional design is evaluated by circuit simulation.
†† Energy/bit is calculated from power dissipation and max bandwidth.
††† Area excludes the contact pads, decoupling capacitor and the output buffer.

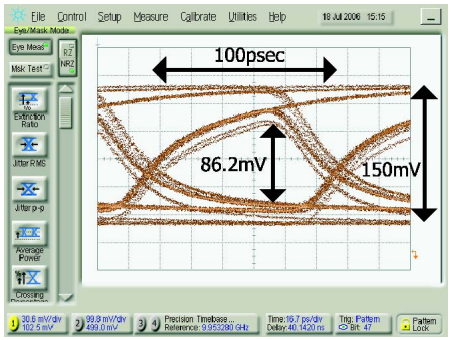

Fig. 6. The eye-diagram at 10GHz PRBS input.

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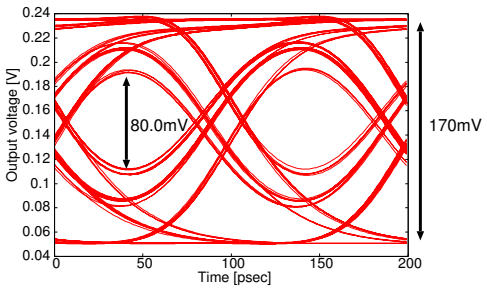

Fig. 7. The eye-diagram at 10Gbps by circuit simulation.