A Multi-Drop Transmission-Line Interconnect in Si LSI

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Abstract — This paper proposes a branching method for on-chip transmission line (TL) interconnects, which can reduce delay and power of global interconnects. A 6-mm-long TL interconnect with a branch is fabricated by using a 0.18 μm standard Si CMOS process, and the measurement result performs 4 Gbps signal transmission.

I. Introduction

Global interconnect delay to a clock period has been continuously increased as technology node advances and has limited performances of Si LSI. On-chip transmission line (TL) interconnects have been investigated to overcome the issue [1]–[6]. It is expected that TL interconnects reduce delay of global wires and can also save the power of LSI [1]. The conventional on-chip TL interconnects are peer-to-peer ones. Many on-chip connections require branches so it is crucially important to develop a branching method for the on-chip TL.

This paper proposes the on-chip TL interconnect with branches. Branching techniques have been discussed for the on-board TLs. The contribution of this work is to apply the idea to the on-chip interconnection and develops a novel circuitry for the branching TL. The measurement result of the proposed circuit is presented, and feasibility of the circuit is discussed.

II. Branching Circuitry of Transmission Lines

Figure 1 shows branching structures for TLs. The structure shown in Fig. 1 (a) has one branching node and two output TLs. As TLs have the same characteristic impedance Z_0 as shown in Fig. 1 (a), input impedance of parallel transmission-lines becomes half of Z_0. Thus, the impedance mismatch is caused, and reflection at the branching node degrades signal integrity. To adjust characteristic impedance, series resistor is often inserted to a branching part of on-board TL. However, the series resistor degrades signal attenuation, which is large disadvantage for the on-chip TL. In a Si CMOS chip, it is feasible to use a short branching line without the series resistor because the on-chip branch line is usually not so long as signal wave length. The reflection can be neglected if branching line is short and input impedance of Rx is large sufficiently.

The proposed branching method is shown in Fig. 1 (b). One of the outputs is connected to the gate of transistor. The branch-line length and the gate capacitance have large influence on signal transmission, which are optimized to obtain higher signal transmission.

Figure 2 shows a test circuit to evaluate effects due to gate capacitance of a branching transistor. CMOS-type Tx, common-source Rxs, and a single-ended transmission line (STL) are used. In this simulation, transistors at branching nodes are modeled as capacitors. Parameters of 0.18 μm CMOS process are used. The length of STL is 6 mm. Lossless characteristic impedance of the STL is 50 Ω, and a line width is 2.4 μm. The STL is terminated by resistor, and capacitors are connected at intervals of 1 mm. Circuit characteristics were evaluated by circuit simulator (Agilent, Advanced Design System).

Figure 3 shows delay from "In" to "OutA" and eye-height at "OutA" in Fig. 2 as a function of total input capacitance of Rx's at 8 Gbps. Delay and eye-height degrade as capacitance increases. When the acceptable degradation of eye height is assumed 5 %, the total gate capacitance of 75 fF can be connected to the STL. In this case, delay is increased by 20 ps. Gate widths of Rxs are required to be 5 μm for amplifying the signal, and gate capacitance is 5 fF in this process. Thus, sixteen Rxs can be distributed to 6-mm-long TL with limited length of branching lines. If sixteen signals are transmitted by using sixteen peer-to-peer interconnects, power of Txs and interconnect area become sixteen times larger than the proposed interconnect. The proposed multi-drop STL interconnect has big advantages of power and area.

Figure 4 shows simulated eye-patterns at Rx outputs of 2 mm and 6 mm. The simulation results show that signals can transmit through the proposed interconnect although deterministic jitter is appeared.

III. Measurement Results

A TL interconnect that has one input and two outputs is fabricated by using a 0.18 μm Si CMOS process. Figure 5 shows the chip micrograph, and Fig. 6 shows a schematic. The length of STL is 6 mm, and Rxs are connected to the STL at center (3 mm) and far-end (6 mm). A microstrip-type STL is used. Signal and ground lines are routed using metal layer 5 and 1, respectively. Thicknesses of metal and dielectric are about 1 μm. Lossless characteristic impedance of STL is 50 Ω, and the width of signal line is 8.0 μm. The transmission characteristics of the proposed interconnect were investigated by time-domain measurements. Figure 7 shows output eye-patterns of Rx at 3 mm and 6 mm. The proposed TL interconnect with branch can transmit 4 Gbps signal.

Table I shows delay of the proposed and conventional on-chip interconnects, and the proposed interconnect is the fastest. Figure 8 shows power consumptions of the proposed interconnect that has a Tx and two Rxs, a peer-to-peer differential-transmission-line interconnect [3] and a peer-to-peer RC line [4]. The proposed interconnect achieves the lowest power and delay from 1.5 to 4 Gbps although it has a branch.

IV. Conclusions

This paper proposes an on-chip transmission-line interconnect with branches. The optimizing method of branch line and Rx is presented to avoid signal degradation caused by reflection. In the measurement result, the proposed interconnect realizes 4 Gbps signal transmission, which has one Tx and two Rxs and is fabricated by a 0.18 μm CMOS process. The proposed interconnect achieves lower power and smaller delay than the conventional interconnections, which is expected to overcome delay issue of global interconnects.

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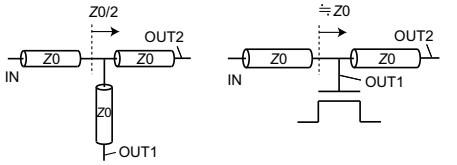


(a) A brute-force branch. (b) The proposed circuit.

Fig. 1. Branching methods for transmission lines.

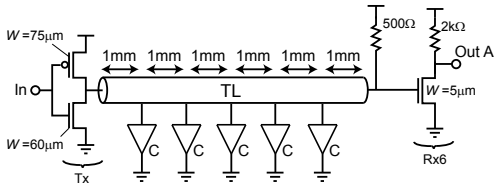
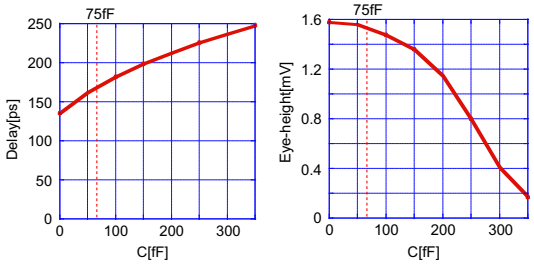


Fig. 2. A test circuit for parasitic capacitance.



(a) Delay. (b) Eye-height.

Fig. 3. Effects of gate capacitance. Signal frequency is 8 Gbps. Horizontal axis show the total capacitance C.

TABLE I

Delay of existing interconnection scheme.

	Delay [ps@1cm]
The proposed interconnect	**144**
Differential transmission line interconnect [2]	185
RC Line [5]	500
Modulation [5]	339
Edge-emitting laser [7]	379
VCSEL [7]	446

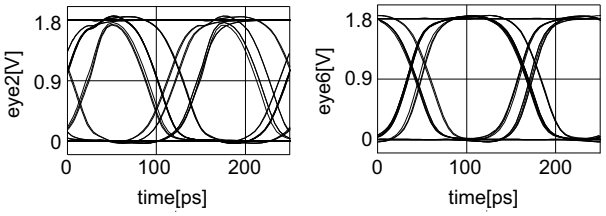


Fig. 4. Eyepattern at 2 mm and 6 mm. Frequency is 8 Gbps.

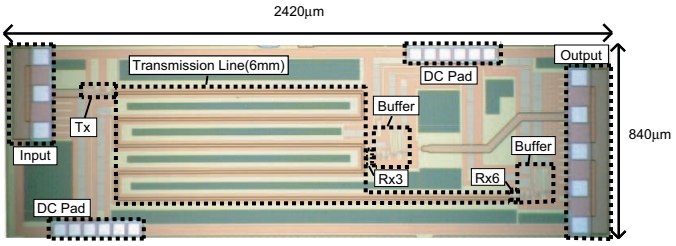


Fig. 5. Chip micrograph.

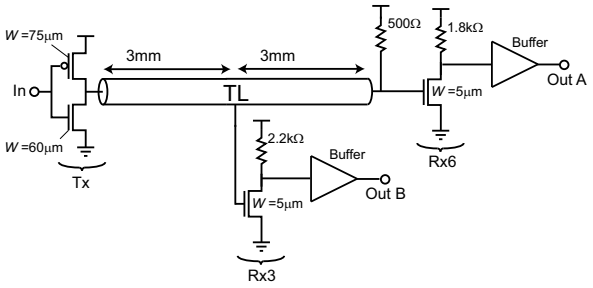
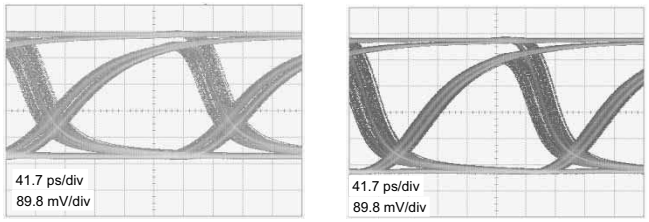


Fig. 6. Schematic of fabricated circuit.



(a) Eye at 3 mm. (b) Eye at 6 mm.

Fig. 7. Eye-pattern (4 Gbps).

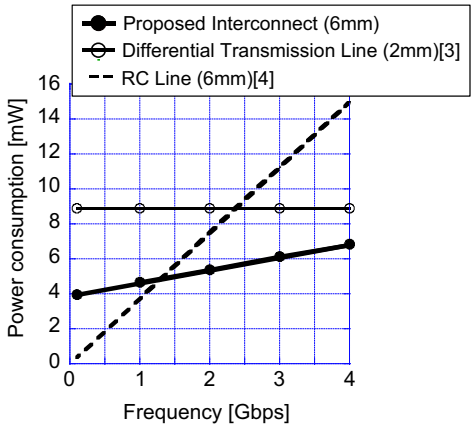


Fig. 8. Comparison of power consumption.