Implementation of a Standby-Power-Free CAM Based on Complementary Ferroelectric-Capacitor Logic

S. Matsunaga†, T. Hanyu†, H. Kimura‡, T. Nakamura‡, and H. Takasu‡

†Research Institute of Electrical Communication, Tohoku University,
2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan
‡New Material Devices R&D Center, ROHM Corporation,
21 Saiin Mizosakicho, Ukyo-ku, Kyoto 615-8585, Japan

Abstract— A complementary ferroelectric-capacitor (CFC) logic-circuit style is proposed for a compact and standby-power-free content-addressable memory (CAM). Since the use of the CFC logic circuit in designing a CAM cell makes it possible to merge both logic and non-volatile storage elements into serially connected ferroelectric capacitors, the CAM becomes compact. The standby power of the CAM is completely eliminated because the supply voltage can be cut off with maintaining stored data in the CAM. The test chip is fabricated by using 0.35-μm ferroelectric CMOS, and the basic behavior can be also measured.

I. Introduction

Parallel search and parallel comparison are the major advantages of CAMs over random access memories. The CAMs are useful as the powerful hardware accelerator in several applications. However, a CAM is more complex to build and has lower storage density than a adrress-based memory because of the overhead involved in the storage, comparison, output selection, and so on. Moreover, its standby power dissipation increases greatly in advanced technology scailing.

In this paper, we propose a compact and standby-power-free CAM based on CFC logic [1]−[2]. In the CFC logic circuit, ferroelectric capacitors are used not only as a non-volatile storage element but also as a logic element, so that the proposed CAM becomes compact. Moreover, its static power dissipation is completely negligible, because ferroelectric capacitors are used as non-volatile storage elements.

II. CFC-logic-based CAM cell design

Fig.1 shows a circuit diagram of the proposed CAM cell to carry out one-bit match. The CAM cell consists of two CFC logic gates each which is a basic element in CFC logic circuits. In the CFC logic gate, a logic function is performed by using capacitive coupling effect between two serially connected ferroelectric capacitors. An important point is that the output voltage V_{out} generated by a capacitive coupling effect depends on the stored data S in the ferroelectric capacitor, because its capacitance depends on the remnant polarization states. In write mode, $\overline{S}$, $\overline{S}$, S, and S are input from the node BL1A, BL1B, BL2A, and BL2B, respectively. As the result, data $\overline{S}$, S, S, and $\overline{S}$ are stored into ferroelectric capacitors FC_1, FC_2, FC_3, and FC_4, respectively, in the definition of positive polarization state as storage data "1", and negative polarization state as "0". In execute mode, complementary input data (X, $\overline{X}$) are applied from the node BL1A and BL2B, respectively. The logic function to carry out one-bit match between X and S can be performed by a wired-AND operation among the outputs of the CFC logic gates as $(X+S)\cdot(\overline{X}+\overline{S})$. The detailed behavior of the CAM cell in execute mode is shown as Fig.2. Fig.3 shows the photomicrograph of the test chip fabricated by using 0.35-μm ferroelectric CMOS, and its measured waveforms, respectively.

III. Implementaion of a CFC-logic-based CAM

Fig.4 shows a block diagram of the CAM and its test chip fabricated by using 0.35-μm ferroelectric CMOS. Match between search word which corresponds to input data "00000010" and previously stored words each which is shifted by one bit from "00000001" to "10000000" can be successfully performed as shown in Fig.5. In case of 8-bit/word configuration, its execution time becomes 25nsec at 3.3V power supply. Moreover, CFC-logic-based CAM can reduce static power dissipation to "0" under the power-off state at the standby mode due to its non-volatility. TABLE I summarizes chip features of the CFC-logic-based CAM.

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IV. Conclusion

We implemented a compact and standby-power-free 8-bit CAM based on CFC logic. Moreover, we fabricated its test chip, and demonstrated the measurement result of the 8-bit match. Since both a logic function and a non-volatile storage function are merged compactly into the CFC logic circuit, it is also expected to realize fine-grain parallel systems.

References

[1] H. Kimura, T. Hanyu, M. Kameyama, Y. Fujimori, T. Nakamura and H. Takasu, "Complementary Ferroelectric-Capacitor Logic for Low-Power Logic-in-Memory VLSI," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp.160-161, February 2003.

[2] H. Kimura, T. Hanyu, M. Kameyama, Y. Fujimori, T. Nakamura and H. Takasu, "Complementary Ferroelectric-Capacitor Logic for Low-Power Logic-in-Memory VLSI," *IEEE Journal of Solid-State Circuits*, Vol.SC-39 No.6, pp.919-926, June 2004.

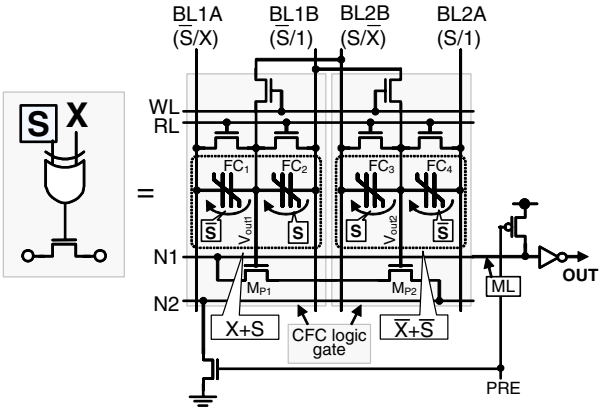
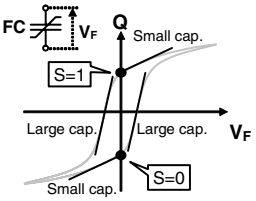


Fig. 1. Circuit diagram of a CAM cell.



Vx (X)	S	FC1, FC4	FC2, FC3	Mp1 (Vout1)	Mp2 (Vout2)	ML
0V (0)	0	Large Cap.	Small Cap.	OFF (V_{low})	ON (V_{high})	1
0V (0)	1	Small Cap.	Large Cap.	ON (V_{high})	ON (V_{high})	0
V_{DD} (1)	0	Large Cap.	Small Cap.	ON (V_{high})	ON (V_{high})	0
V_{DD} (1)	1	Small Cap.	Large Cap.	ON (V_{high})	OFF (V_{low})	1

Fig. 2. Logic operation in a CAM cell.

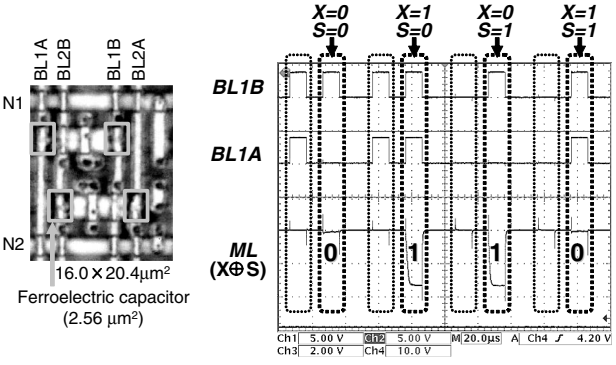


Fig. 3. Test chip and measured waveforms of a CAM cell.

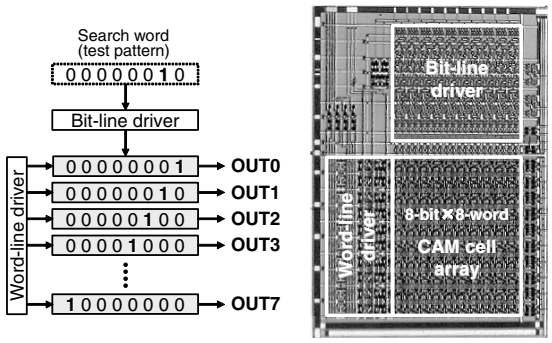


Fig. 4. Block diagram and test chip of a CAM.

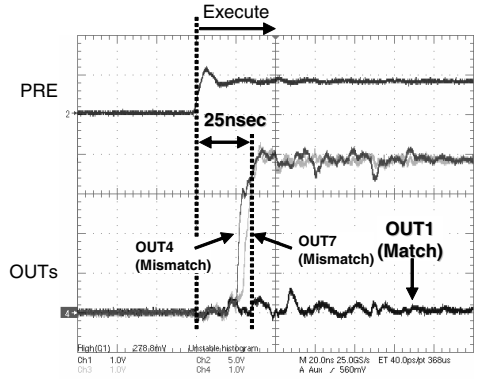


Fig. 5. Measured waveforms of a CAM.

TABLE I
Chip features.

Design rule	0.35μm CMOS / 0.6μm Ferroelectric
Process	1-Poly/1-Metal
Ferroelectrics	PZT
Supply voltage	3.3V
Organization	8-bit×8-word
Execution time	25nsec
Standby current	0A (Power-off)
Capacitor size	2.56μm²
Cell size	16.0μm×20.4μm
Cell structure	8T-4C