Reconfigurable CMOS Low Noise Amplifier Using Variable Bias Circuit for Self Compensation

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***Abstract*— This paper proposes a self compensation technique. For LNAs, large power gain and large input signal results in too large output signal and distortion. To make matters worse, input power varies by process variation, temperature, simulation error, and so on. To solve the problem, the proposed LNA is equipped with variable bias circuit and can be reconfigured by bias voltage of transistors. It contributes to power reduction, compensation of intermodulation. The proposed LNA achieves more than 33 dBm in ΔIM3, if the input power increases more than −30 dBm. Moreover the output power is less than about −12 dBm, which is 87 % of power reduction.**

I. Introduction

Recently, CMOS RF circuits have been developed for mobile wireless terminals. While CMOS circuits achieve higher operating frequency, performance is easily degraded by process variation, simulation error, temperature at the runtime, etc. Therefore, CMOS circuits usually have redundant performance margin to achieve the required performance under every process and runtime conditions, which results in overall performance degradation. To improve the overall performance of RF circuits, we propose the reconfigurable RF circuit architecture [1], [2] for *multiple functionality* and *self compensation*. The multiple functionality provides a multi-band/mode circuit operation for a wireless communication chip, while the self compensation provides the compensation of the circuit performance by dynamic reconfiguration. This paper presents a reconfigurable low noise amplifier (LNA) with the self compensation.

II. Self compensation LNA Using Variable Bias Circuit

Though many compensating mechanisms have been investigated for ADC, DAC, PA, etc, to compensate for process fluctuation, temperature, the modeling error, etc, the proposed reconfigurable RF circuit architecture provides a systematic framework using a digital-control mechanism and more flexible reconfiguration as shown in Fig. 1

Figure 2 shows the circuit schematic of the proposed LNA. The bias circuit consists of current mirror and complementary MOS switches which can tune bias voltage of input transistor. Gain, noise and power consumption depending on the runtime environment are compensated by using the bias circuit, without the redundant design margin [3].

This paper presents the self compensation for input power variation. The main consideration is that large power gain is not required when input-signal power is large. Large power gain and large input signal results in too large output signal, which causes redundant power dissipation and saturation of the next-stage circuit [4].

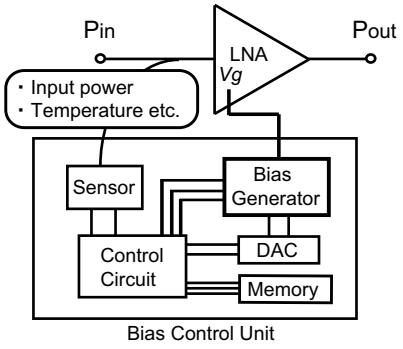

Fig. 1. Architecture of the reconfigurable LNA.

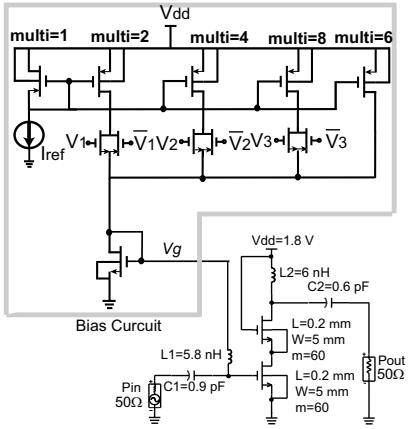

Fig. 2. Circuit schematic of the LNA.

III. Measurements of the LNA

Figure 3 shows a photograph of the LNA fabricated by using a 0.18 μm CMOS process.The measured bias voltage dependence of the LNA is shown in Fig. 4, where ΔIM3 is the deference in output power between desired signal (P_{out}) and 3rd harmonic (IM3). By increasing bias voltage, power gain is improved because g_m varies. ΔIM3 is degraded because power gain is saturated. Power consumption is increased because of larger I_{dd}. NF does not have heavy dependence on the bias voltage. Figure 5 shows input-output power characteristics parameterized by the bias voltage V_g. In this case, we can

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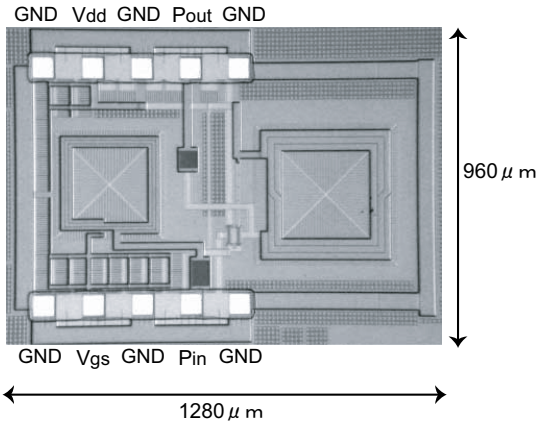

Fig. 3. Photomicrograph of the LNA.

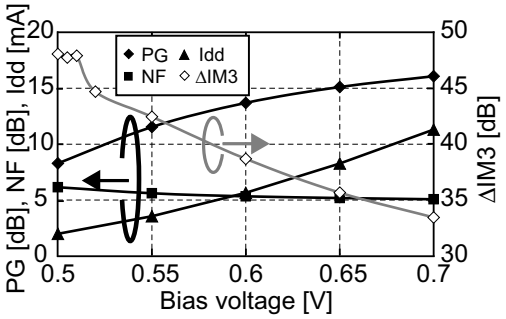

Fig. 4. Measurement result of bias voltage dependence of the LNA.

design a switching scheme as listed in Table I, which aims to compensate for distortion and extra power consumption. The switching scheme can be determined by Fig. 5 and 6 to compensate for the distortion characteristics. To avoid the saturation in the next stage, output-signal power P_{out} is assumed to be less than -12 dBm. To avoid the distortion at the output, ΔIM3 is assumed to be more than 32 dBm. NF is not dominant of bias voltage as shown in Fig. 4. The switching scheme shown in Table I satisfies the above condition.

Figure 7 shows the power consumption. When V_g is 0.7 V, the power consumption of the LNA is about 20 mV, whereas when V_g is lowered to 0.5 V, the power goes down to about 3.6 mV, which is 87 % reduction. The proposed LNA can compensate for the performance degradation and obtain higher balanced performance.

IV. Conclusions

This paper proposes a reconfigurable low noise amplifier (LNA) using variable bias circuit. The measurement results show the proposed LNA has lower power consumption, and higher ΔIM3 as compared to a conventional LNA. Furthermore, the proposed LNA can save the design cost because redundant design margin is not required for the worst-case condition. The dynamic reconfigurable technique can become a promising technology for the future RF circuit design.

Acknowledgement

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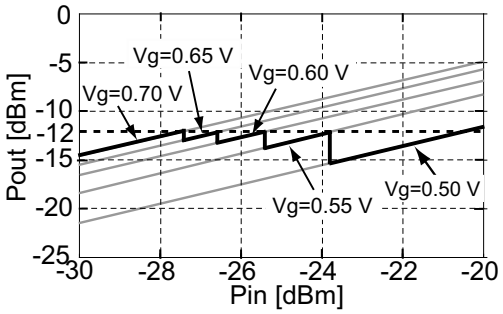

Fig. 5. Measurement result of output power of the LNA.

TABLE I
Switching scheme

P_{in} [dBm]	$\Downarrow$ -27.4	-27.4 $\Updownarrow$ -26.6	-26.6 $\Updownarrow$ -25.4	-25.4 $\Updownarrow$ -23.8	-23.8 $\Downarrow$
V_g [V]	0.70	0.65	0.60	0.55	0.50

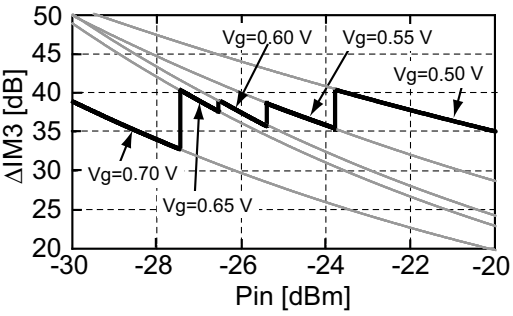

Fig. 6. Measurement result of Δ3rd-order intermodulation (ΔIM3) of the LNA.

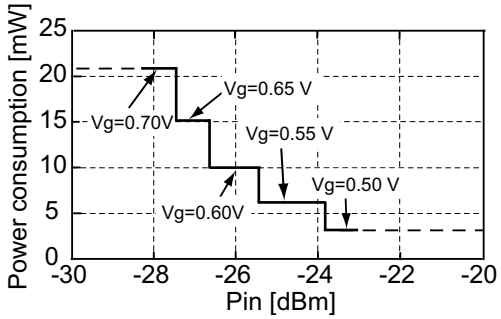

Fig. 7. Measurement result of power consumption of the LNA.

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