Design of Active Substrate Noise Canceller using Power Suplly di/dt Detector

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Abstract— As the growing demand of mixed-signal designs as A/D, D/A and PLL integrated with large scale digital circuits, substrate noise becomes serious concern. On the other hand, the remedies using guard ring and decoupling capacitor do not have enough efficiency against high frequency noise due to their parasitic component. To suppress the impact of substrate noise, on-chip active noise cancelling technique using di/dt detector has been proposed[1][2][3]. This paper introduces an exapmle design of feedforward active substrate noise canceling technique using multiple power supply di/dt detector and demonstrates the noise cancelling results by the measurement of 0.35 μm CMOS test chip.

I. Introduction

The main cause of substrate noise is a coupling from digital ground lines. At higher frequency, ground bounce is affected by inductance ($L_{gnd}(di/dt)$) of power/gnd line strongyly. Substrate noise is, therefore, proportional to di/dt. From this kind of background, an active substrate noise canceller is realized by di/dt detection. A di/dt detector was proposed in [1], and the detailed structure of di/dt detector circuits is shown in figure 1. A power supply current of the internal circuit goes through parasitic inductance L_1 of the power supply line. A pickup inductance L_2 of di/dt detector coupled to L_1 with a coupling coefficient K induces a di/dt propotional voltage. A noise tolerant amplifier amplifies the induced voltages and generates anti-phase di/dt proportional current. This di/dt detector can be applicable to cancelling the substrate noise by injecting anti-phase noise current into substrate. A standard block diagram of feedforward active substrate noise canceling system is shown in figure 2. If the anti-phase noise signal is injected into substrate, the original substrate noise can be canceled out.

II. Design of DI/DT Canceller

The inductance L_1 should be small since it is series connection to the power supply line. The small inductance requires a high coupling coeffcient K and a larger L_2 in order to generate sufficient cancelling signal against original substrate noise. High frequency, high linearity and appropriate phase characteristics are the key design issues for the di/dt canceller.

Characteristics of the noise canceller depend on two component: characteristic of amplifier and LRC low pass filter of

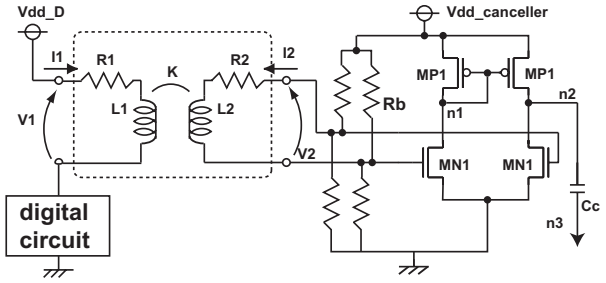

Fig. 1. Circuit design of di/dt detector.

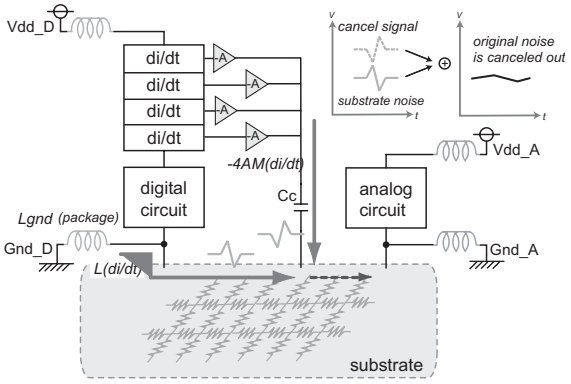

Fig. 2. Design diagram of active substrate noise canceller using power line di/dt detector.

noise detector. Here, the input impedance of the substrate from the injection point is assumed to be pure resistive. This low impedance output helps realization of wide bandwidth of the canceller. The secondary inductance L_2, R_2 and the input capacitance of the amplifier MN_1, MN_2, form LRC low pass filter, whose characteristic is given by L_2 and MN_1/MN_2. (1) $f_{target} \ll f_L = 1/(2\pi\sqrt{C_g L_2})$. (2) $f_{target} \ll f_R = 1/(2\pi C_g R_2)$. Where L_2, R_2 are inductance and resistance of secoundary inductace respectively , and Cg is gate capacitence of the amplifier. The noise cancelling signal should be small against substrate noise to meet these characteristics of the canceller. Therefore, we employ multiple di/dt cancellers for further substrate noise suppression. The multiple di/dt cancellers with

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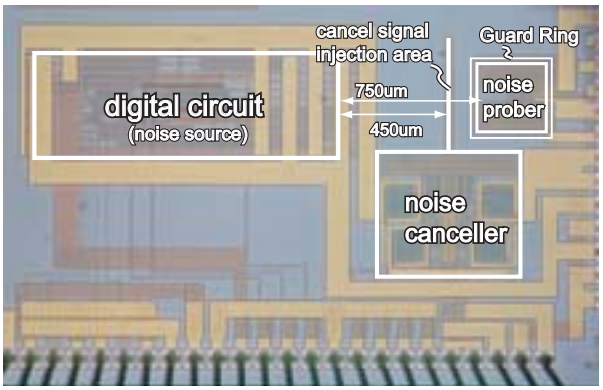

Fig. 3. Chip microphotograph of the multiple di/dt canceller using 0.35μm CMOS technology. The area is 3.0mm × 1.8mm

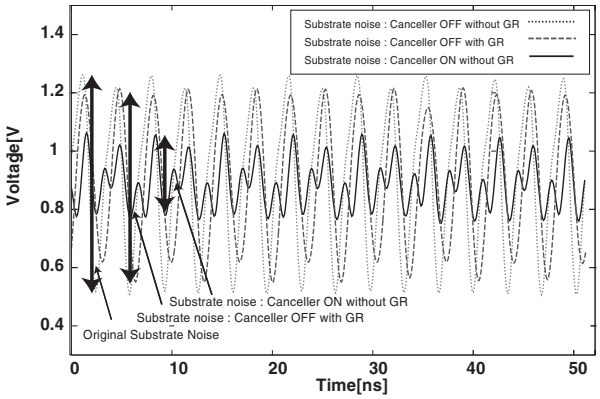

Fig. 4. Waveform of substrate noise with canceller on and off.

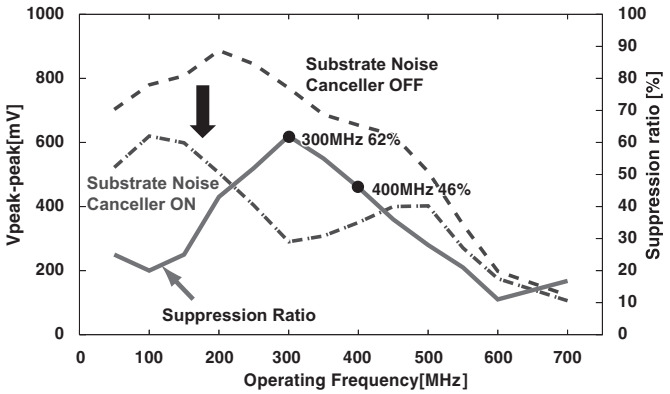

Fig. 5. Frequency characteristics of multiple di/dt noise canceller.

appropriate frequency characteristics can inject larger current without large phase shift. Figure 3 shows a chip photograph of the multiple di/dt cancellers fabricated using 0.35 μm CMOS technology. The chip area is 3.0mm × 1.8mm. The substrate noise probing point to measure substrate noise at victim (analog circuit) is located 750μm apart from the noise source, and the cancel signal injection area is located between the noise source and the probing point.

III. Measurement of Substrate Noise Waveforms

The measured waveforms of the substrate noise signals with noise cancller on and off are shown in figure 4. We adjusted the gain of canceller by sweeping the power supply voltage of the canceller and detected the most effective point (minimum peak-to-peak of substrate noise). The operating frequency is 300MHz, and the gain of noise probe at this frequency is 7.5 by HSPICE simulation. This graph shows that 62% substrate noise are suppressed by using multiple di/dt cancellers if the peak-to-peak voltages are concerned. Figure 4 also shows the measured waveforms of substrate noise with/without guard ring. Guard ring is placed nearby noise probe which is assumed as an analog circuit. Guard ring suppresses the 13.4% substrate noise at 300MHz. Note that the multiple di/dt canceller can suppress substrate noise more effectively than the guard ring. Figure 5 shows the measurement results of frequency characteristic of di/dt noise canceller. The frequency characteristic shows the multiple di/dt canceller realize 10-60% noise suppression for 100-700MHz.

IV. Conclusion

Active substrate noise canceling technique using multiple di/dt cancellers has been demonstrated. Our active canceling technique detects the di/dt of the power supply current and injects an anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. The measuremet results show that 62% of the substrate noise reduction was achieved in our 300MHz operating test circuit fabricated using 0.35 mum CMOS technology. Multiple di/dt cannceller has as five times noise reduction effect as that of guard ring. In addition, multiple di/dt canceller realize 10-60% noise suppression for 100-700MHz.

The area overhead of the presented di/dt canceller is dominated by the pickup inductance in the conventional 0.35μm CMOS design. This area overhead, however, will be shrinking in the advanced technologies, since the di/dt on power line increases in proportion to the operating frequency.

Acknowledgements

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