Utility of the OpenAccess Database in Academic Research

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ABSTRACT

The proliferation of OpenAccess is opening promising new research opportunities to academic communities. The benefits of adopting an OpenAccess based approach to EDA research are growing, and we review a number of them. Among them are the ability to learn about a domain while writing software for it, increased ease of code reuse, new high-quality benchmarks, and enhanced industry adoption.

1. INTRODUCTION

Twenty years ago, there was a common design tool which was free and open-source and satisfied the needs of many academic circuit designers. The Magic VLSI Layout System introduced at DAC in 1984 [7] was an effective solution that enabled academic designers to comply with design rules of that time. However, the size of designs and complexity of design rules has increased drastically since then, and the strain created a need for newer more scalable tools. To enable collaboration one needs a common database, but maintaining software to handle the increased complexity in one academic group is hopeless. Given the amount of investment necessary to develop a single integrated approach, one can only hope to accomplish this task with the help of industry. CAD Framework Initiative, Inc. was formed in 1988 to organize these efforts [3]. Unfortunately, this work never took off, and until recently all major EDA companies had their own proprietary data models that were developed to support their specific flows. OpenAccess is a new attempt at the same goal and aims to meet the needs of everyone. CAD Framework Initiative is now known as SI2 [8] – an organization of industry-leading silicon systems and tool companies that maintain the OpenAccess standard. The collaborative technology developed by SI2 benefits academic researchers in a number of ways.

2. EDUCATIONAL PROTOTYPING

OpenAccess is a featureful data model which has been designed to efficiently perform the operations of typical VLSI design tasks. This should be leveraged when developing new algorithms, but is particularly helpful for prototyping.

Often in research, the easiest way to evaluate an optimization is to implement it and measure its impact empirically. When these optimizations are not helpful or cost-effective (e.g. too slow) they are abandoned in favor of a more promising direction. Therefore it is desirable to quickly develop prototypes that can be used to extrapolate if an optimization is viable.

To support academic prototyping efforts, the free, open-source OpenAccess Gear toolkit provides several useful EDA components, such as an incremental static timing analysis tool and an interface to the Capo placement engine [6]. Such tools allow users to use OpenAccess to build complex flows on top of OpenAccess which would otherwise be difficult or costly to implement in an academic environment, such as timing-driven placement flows. Recently several new features have been added to OpenAccess Gear, including a logical representation layer, which allows academics to build physically-driven synthesis tools on top of OpenAccess. Such an ability to inexpensively and rapidly prototype interesting tools in universities is made possible only due to the open nature of OpenAccess and OpenAccess Gear.

3. CODE REUSE

One of the greatest motivations for development in OpenAccess is the increased ease of code reuse. Once a *service* or *transformation* of a VLSI design is defined for the OpenAccess data model, it can be used as a part of larger OpenAccess-based applications without costly conversions from one data representation to another. Such straightforward reuse is particularly attractive to academia because it avoids the burden of extending home-grown data models to efficiently handle the operations of new algorithmic components brought in from 3rd party sources.

One prominent case of this type of reuse is in the creation of a timing-driven version of the Warp placer [9]. Xiu et al. estimate that the development effort was reduced from 3 months to 1 month by the ability to reuse the OpenAccess Gear timer. Because of the incremental nature of timing queries in the process of placement, using a standalone timer would not be adequate. Rather, calls to the timer must be integrated into placement. Since Xiu et al. were able to reuse timer code, they saved themselves the effort of writing a timing analyzer required for timing-driven placement.

4. HIGH-QUALITY BENCHMARKS

The reported improvements in many physical design papers are so small that it is necessary to check improvements against additional realistic designs. To this end, the importance of a diverse set of high-quality benchmarks has been demonstrated for VLSICAD tools [1]. That work notes several problems with open benchmark suites such as designs that are too small, artificially constructed, or missing important information.

Many of these problems are addressed in a new open suite of designs in the OpenAccess and Verilog formats [5]. This suite contains 84 real designs with up to 185k registers and 900k gates. All designs are mapped with Cadence RTL Compiler to a 180nm library which is included in the suite. Using a tool that comes free with OpenAccess Gear [6], physical information is generated for these designs including core area, core rows and routing tracks. In addition, much of the information which has been lost in previous benchmark suites is preserved for these designs, such as signal directions of nets and logic information of cells. The presence of this information enables new experiments of interest to the academic community. For example, signal directions allows one to examine and optimize signal paths, and logic information allows for detecting equivalence of signals – also useful in circuit optimization. This information is available in some small benchmarks, but not on large realistic designs.

5. INDUSTRY ADOPTION

The International Technology Roadmap for Semiconductors [2] calls for a shift in the architecture of VLSI design systems into an

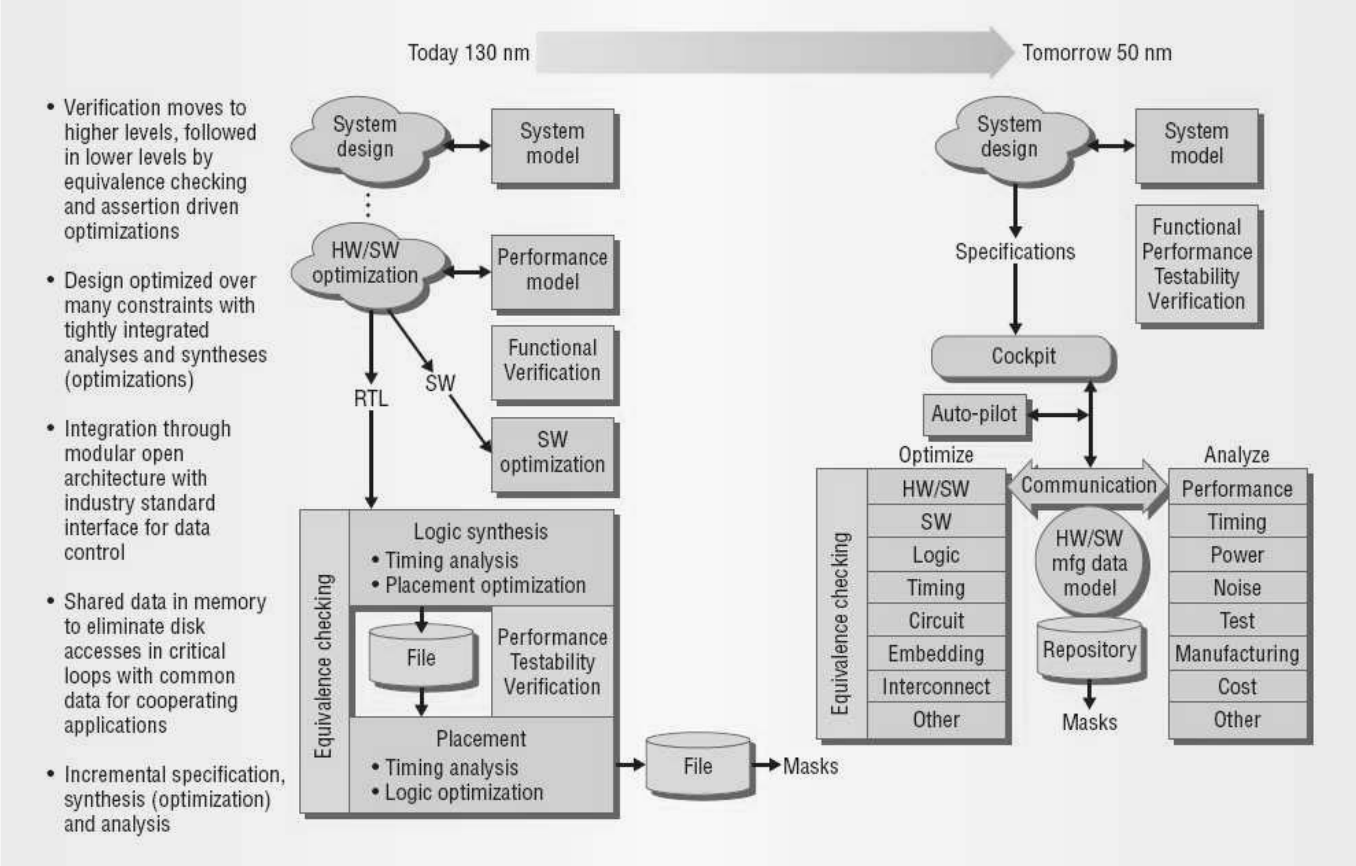

Figure 1: This figure from the 2001 ITRS shows that as tools become more interoperable, design system architecture will change toward a more integrated approach. OpenAccess is one example of the Repository in the architecture at 50nm.

integrated system of interoperable tools. Central to this theme is a single data model used by all tools, with analysis tools used to drive optimization steps. Figure 1 shows how design system architecture will evolve with increased tool interoperability. OpenAccess is likely to lead the way in this worthwhile paradigm shift. Until recently this functionality was unavailable to academia due to lack of infrastructure. With OpenAccess, a flow similar to the right flowchart of Figure 1 is possible. This allows research on reordering of optimization steps of traditional VLSI design flows, e.g., applying logic optimization after placement [4].

Industry partners will be much more likely to adopt research software that works with the same data model, and is built using the same architecture as their commercial tools. This is mutually beneficial because it allows industry to reap immediate benefit from new research, and thus benefits academic research by encouraging industry to support it.

6. CONCLUSIONS

OpenAccess brings many benefits to academic researchers including improved open benchmarks, easier code reuse, faster prototying and enhanced industry adoption. However, there are some downsides associated with adopting an approach using OpenAccess. Converting established software to run natively on OpenAccess can be a huge endevour. Additionally, since many academic groups distribute open-source software, licensing conflicts can arise with OpenAccess. This is because many open-source licenses are less restrictive than the current OpenAccess license which can restrict users of open-source software. This means that supporting OpenAccess in open-source software is likely to be an addition to, rather than as a substitution for existing data models.

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